various numbers of capacitors being switched into the circuit. The intersection of the vertical line extending through V_L and the horizontal line extending from 900 MHz defines the point at which lock is desired. Using a well defined V_L, has the problem that control voltage may be swept along a capacitance curve and past the lock point without producing a lock. The process would then switch capacitance in or out of the circuit causing a jump to a new curve of the family tending to pass the lock point without locking the PLL. Hysteresis tends to force the process to hunt along the presently selected curve for a slightly longer time to ensure that the PLL locks while on the correct capacitance curve.

FIG. 47d is a graph of a family of frequency verses control voltage for various capacitor values that illustrates the use of dual comparator windows to aid in achieving a frequency lock condition. The graph illustrates the sliding window of valid lock ranges provided by the design. A valid lock range for a low V_{GT} and a high V_{GT} are shown. The voltage range of the window is constant. However, the starting and ending values of the window vary.

Once the fine, or narrow band PLL has been tuned such that is has been locked its frequency may be used in conjunction with the frequency generated by the coarse PLL to provide channel tuning as previously described for the coarse/fine PLL tuning of FIGS. 21 and 22.

RECEIVER

FIG. 48 is a block diagram of a first exemplary embodiment of a receiver. FIGS. 48, 51, 52, 53 and 54 are embodiments of receivers that utilize band pass filters and image reject mixers to achieve image rejection that tend to reduce the distortion previously described. The embodiments advantageously convert an input signal (1906 of FIGS. 19, 48, 51, 52, 53 and 54) to a final

IF frequency (1914 of FIGS. 19 48, 51, 52, 53 and 54) by processing the input signal substantially as shown in FIG. 19. Image rejection is measured relative to the signal strength of the desired signal. The strength of the unwanted image frequency is measured in units of decibels below the desired carrier (dB_c). In the exemplary embodiments of the invention an image frequency rejection of 60 to 65 dB_c is required. In the embodiments of the invention this requirement has been split more or less equally among a series of cascaded filter banks and mixers following the filters. The filter banks 1912,1934 provide 30 to 35 dB_c image rejection and complex mixers 4802,4806 used provide an additional 30 to 35 dB_c of image rejection yielding an overall image rejection of 60 to 70 dB_c for the combination. The use of complex mixing, advantageously allows the rejection requirements on the filters to be relaxed. First, a channel of an input spectrum is centered about a first IF frequency.

FIG. 49 is an exemplary illustration of the frequency planning utilized in the embodiments of the invention for the reception of CATV signals. The frequency spectrum at the top of the figure 4902 illustrates exemplary received RF signals ranging from 50 to 860 MHz 4904. The received RF signals are applied to a band pass filter 4921 to eliminate out of band distortion products Image1 4906. The frequency plan advantageously utilizes a trade off between image rejection achievable by filters and mixers at different frequencies. The processing of the first IF and the second IF have many features in common and will be discussed together in the following paragraphs.

For example, the second mixer 4802 and second bank of IF filters 4834 of FIG. 48 achieve 35 dB and 35 dB of image rejection, respectively. The third mixer 4806 and the third IF filter bank 1936 of FIG. 48 achieve 25 dB and 40 dB of image rejection respectively. The last distribution reflects the fact that at the lower third IF frequency the Q of the filters tend

to be lower, and the image rejection of the mixers tend to be improved at lower frequencies.

For example, returning to FIG. 48, a signal 1906 in the 50 to 860 MHz range is up converted by mixer 1916 and LO2 1908 to 1,200 MHz IF-1 1918. The presence of LO-2 1904 at 925 MHz that is required to mix the signal IF-1 1918 down to the 275 MHz IF-2 1922 has an image frequency Image2 (4908 as shown in FIG. 49) at 650 MHz. The filter Q of the 1,200 MHz center frequency LC filter 1912 causes Image2 to undergo 35 dB of rejection thus, attenuating it. To achieve 70 dB of image rejection another 35 dB of rejection must be provided by the second mixer (4702 of FIG. 48) that converts the signal from 1,200 MHz to 275 MHz.

Continuing with FIG. 48, the same structure as described in the preceding paragraph is again encountered, but at a lower frequency for the second IF 4914. Image rejection of the 275 MHz filter (1934 of FIG. 48) is less due to its lower Q and the fact that the image frequency Image3 4912 is spaced only 88 MHz 4910 from the signal IF-2 4914. In the previous first IF stage the image frequency Image2 4908 was spaced 550 MHz 4918 from the signal IF-1 4916, providing better image attenuation by filter stop bands. In this situation 25 dB of selectivity can be achieved in the filter, requiring 40 dB of rejection in the mixer to achieve at least 65 dB of attenuation of Image3.

Phase matching at lower frequencies is more accurate allowing better image rejection to be obtained from the third mixer. The method of trading off filter selectivity against mixer image rejection at different frequencies advantageously allows a receiver to successful integrate the filters on chip with the desired image frequency rejection. This process is described in detail in the following paragraphs.

Returning to FIG. 48, it is desired to up convert a channel received in this band of signals 1906 to a channel centered at

an intermediate frequency of 1,200 MHz 1918. A local oscillator 1908 produces frequencies from 1,250 MHz to 2060 MHz. For example, a channel centered at 50 MHz is mixed with the local oscillator set at 1,250 MHz to produce first IF frequency components 1918 at 1,200 MHz and 1,300 MHz. Only one of the two frequency components containing identical information produced by the mixing process is needed; the low side 1,200 MHz component is kept. Filtering 1912 tends to remove the unneeded high side component and other desired signals.

Choosing the first IF 1918 to be centered at 1,200 MHz makes the first IF susceptible to interference from a range of first image frequencies from 2,450 MHz to 3,260 MHz (4906 as shown in FIG. 49), depending upon the channel tuned. The lower image frequency of 2,450 MHz results from the first IF of 1,200 MHz being added to the lowest first LO present at 1,250 MHz to yield 2,450 MHz. The highest image frequency results from the first IF of 1,200 MHz being added to the highest first LO of 2,060 MHz to yield 3,260 MHz as the highest first image. Choosing the first IF 1918 at 1,200 MHz yields image frequencies (4906 of FIG. 49) that are well out of the band of the receiver. The result tends to place undesired frequencies far down on the filter skirts of filters present in the receiver, attenuating them.

After a channel is up conversion to a first IF 1918 of 1,200 MHz, it is next filtered by a bank of 3 LC band pass filters 1912 each having its response centered at 1,200 MHz in the embodiment. These filters in conjunction with the second mixer 4802 provide 70 dB of image frequency rejection (4908 of FIG. 49). Filters are advantageously integrated onto the CMOS substrate. An LC filter comprises inductors (or coils) and capacitors. An inductor implemented on a CMOS substrate tends to have a low Q. The low Q has the effect of reducing the selectivity and thus the attenuation of signals out of band.

The attenuation of signals out of band can be increased by cascading one or more filters. Cascading filters with identical response curves has the effect of increasing the selectivity, or further attenuating out of band signals. The embodiments of the invention advantageously incorporate active g_m stage filters 1912,1934 to increase selectivity and provide circuit gain to boost in band signal strength. Three cascaded active LC filters implemented on a CMOS substrate yield a satisfactory in band gain, and provide approximately 35 dB of out of band image signal rejection in the embodiment described. However, the filters need not be limited to active LC filters, other characteristics and passive filters are contemplate equivalents.

The remaining 35 dB of image frequency rejection needed must be achieved in the other circuitry. Hence, differential I/Q mixers 4802,4806 are advantageously used to achieve this approximate 35 dB of additional image rejection required in the first IF.

FIG. 50 is a block diagram illustrating how image frequency cancellation is achieved in an I/Q mixer. An I/Q mixer is a device previously developed to achieve single side band signal transmission. It is one of three known methods for eliminating one of two side bands. This type of mixer is able to transmit one signal while eliminating or canceling another signal. An I/Q mixer advantageously possesses the properties of image frequency cancellation in addition to frequency conversion. For example, returning to FIG. 48, a second LO 1904 of 925 MHz is used to create the down conversion to a second IF 1922 of 275 MHz, while rejecting image frequencies from the previous frequency conversion by LO1 1908.

The I/Q mixers are implemented in several ways in the invention. However the overall function is maintained. An interconnection of components that achieves I/Q mixing is illustrated in the exemplary I/Q mixer 4802 shown in FIG. 48.

First an input signal 1918 is input to a mixer assembly comprising two conventional mixers 4828, 4830 of either a differential (as shown) or single ended construction.

Local oscillator signals 1904, that need not necessarily be buffered to achieve I/Q mixing, are applied to each mixer. The local oscillator signals applied to each mixer are of the same frequency, but 90 degrees out of phase with each other. Thus, one signal is a sine function, and the other is a cosine at the local oscillator frequency. The 90 degree phase shift can be generated in the I/Q mixer or externally. In the circuit of FIG. 48 a conventional poly phase circuit 4832 provides the phase shift and splitting of a local oscillator signal generated by PLL2 4806.

Two IF signals, an I IF signal and a Q IF signal, are output from the mixers and fed into another conventional poly phase circuit 4834.The poly phase circuit outputs a single differential output IF signal.

Returning to FIG. 50, the I/Q mixer uses two multipliers 5002,5004 and two phase shift networks 5006,5008 to implement a trigonometric identity that results in passing one signal and canceling the other. The trigonometric identity utilized is:

$$\cos(2\pi f_{RF}t)\cos(2\pi f_{LO1}t) \pm \sin(2\pi f_{RF}t)\sin(2\pi f_{LO1}t) = \cos[2\pi(f_{RF} - f_{LO1})t] \quad (8)$$

where f_{RF} is an input signal 5010
f_{LO1} is the first LO 5012

The signals produced and blocks showing operations to create signal transformation of these signals to yield the desired final

result is shown in FIG. 50. The process makes use of a hardware implementation of the trigonometric identities:

$$\sin(u)\sin(v) = \tfrac{1}{2}[\cos(u-v)-\cos(u+v)] \quad (9)$$

and

$$\cos(u)\cos(v) = \tfrac{1}{2}[\cos(u-v)+\cos(u+v)] \quad (10)$$

By applying these trigonometric identities to the signals created by the two mixers, the product of the sine waves 5014 is:

$$\tfrac{1}{2}[\cos(2\pi f_{LO1}t - 2\pi f_{RF}t) - \cos(2\pi f_{LO1}t + 2\pi f_{RF}t)] \quad (11)$$

and the product of the cosines 5016 is:

$$\tfrac{1}{2}[\cos(2\pi f_{LO1}t - 2\pi f_{RF}t) + \cos(2\pi f_{LO1}t + 2\pi f_{RF}t)] \quad (12)$$

Thus, two frequencies are created by each multiplication. Two of the frequencies have the same sign and frequency, so that when they are added together 5018 the resultant signal is a positive sum 5020. The other frequency created cancels itself out 5022. The sum frequency component created by the product of the sines is a negative quantity. The same sum frequency component created by the multiplication of the cosines is positive and of equal magnitude. Thus, when these signals are added together one frequency component, the difference, that is present in each signal has twice the amplitude of the individual signals and the second, sum frequency created is of opposite polarity of the other signal created and cancels out when the signals are added together. Thus, the difference frequency is passed to the output while the sum frequency component is canceled.

The implementation of this trigonometric identity by a circuit is very useful for canceling image frequencies. As shown

in FIG. 4 signal, S and image signal I are equally spaced by the IF frequency from the local oscillator frequency. The signal frequency would be represented by the term $(2\pi f_{LO1}t - 2\pi f_{RF}t)$ and the image frequency would be represented by $(2\pi f_{LO1}t + 2\pi f_{RF}t)$. In the embodiments of the invention, the phase shifting and summing functions are performed utilizing standard polyphase or other circuits known in the art.

Mathematically exact cancellation can be achieved. However, real circuit components are not able to achieve exact cancellation of the image frequency. Errors in phase occur in the circuitry. A phase error of 3° can yield an image frequency suppression of 31.4 dB_c and a phase error of 4° can yield an image frequency suppression of 28.9 dB_c. These phase errors tend to be achievable in an integrated circuit on CMOS. To attempt to achieve the entire 70 dB_c of image rejection tends to be undesirable, thus necessitating the filters. For example, to achieve 59 dB_c of image frequency rejection a phase error tending to be of no more than 0.125° in the mixer would be allowable.

By combining image frequency rejection achievable by an LC filter implemented in CMOS with an I/Q mixer's image rejection properties, properties that tend to be achievable in a CMOS integrated circuit, a required image frequency rejection is obtained. Additionally, the frequency of a first up conversion has been advantageously selected to place an image frequency of a first LO well down the filter skirts of a 1,200 MHz LC filter bank, thus achieving the desired image frequency rejection.

Returning to FIG 48, buffer amplifiers 4810 are used to recondition the amplitudes of LO signals 1908,1904,1930 that drive the I/Q ports of mixers 4802,4806. A distance of several millimeters across a chip from where LOs are generated 4504,4506,4508,4502 to where it is applied at the mixers 1916,4802,4806 tends to require reconditioning of the slopes of

the local oscillator signals. Buffering also tends to prevent loading of the PLLs 4504,4806.

Eliminating any preselection filtering requiring tunable band pass filters is desirable. To do this image frequency response and local oscillator (LO) signals are set to fall outside of a received signals bandwidth. The first signal conversion tends to eliminate any requirements for channel selectivity filtering in the receiver front end. Because of the integrated circuit approach to this design it is desirable to locate an LO outside of the signal bandwidth to reduce distortion created by the interaction of the received signals and the first local oscillator signals.

An approximately 35 dB of out-of-band channel rejection in the first IF stage's filter 1912 is insufficient. The additional 35 dB of selectivity provided by a mixer 4802 increases selectivity. However, it is desirable to mix down a received signal as quickly as possible. This is desirable because at lower frequencies filters tend to have better selectivity than at the higher IF frequencies. By converting a received signal to as low a frequency as possible as quickly as possible better filtering tends to be obtained. Two frequency down conversions are next performed.

Filters are available that will achieve a better rejection than an LC filter at a given frequency, for example a SAW filter. While better filtering of the intermediate frequencies could be obtained with a filter such as a SAW filter at a higher frequency, a fully integrated receiver would not be achievable. A SAW filter is a piezoelectric device that converts an electrical signal to a mechanical vibration signal and then back to an electrical signal. Filtering is achieved through the interaction of signal transducers in the conversion process. A filter of this type is typically constructed on a zinc oxide (ZnO_2), a material that is incompatible with integration on a

CMOS circuit utilizing a silicon (Si) substrate. However in alternative embodiments of the invention, SAW or other filter types known in the art including external LC filters are contemplate embodiments. In particular, a hybrid construction utilizing receiver integrated circuit bonded to a hybrid substrate and filters disposed on the substrate is contemplated.

Returning to the frequency plan of FIG. 49, there is an image response (Image2) 4908 associated with the second local oscillator signal (LO_2) 4920. Returning to the embodiment of FIG. 48, this Image2 signal occurs at $f_{LO2} - f_{IF2}$ = 925 MHz - 275 MHz, which is 650 MHz. If there is a signal of 650 MHz at the receiver's input 4808 it is possible that a 650 MHz signal will be mixed down to the second IF frequency (IF_2) (1922 of FIG. 48) causing interference with the desired received signal which is now located at the second IF frequency. To reduce interference from this signal the receiver has been designed to produce greater than 65 dB of rejection of Image2 by the mechanism previously described for the 1,200 MHz LC filter bank 1912 of FIG. 48.

Returning to FIG. 48, the third IF is next generated. The third LO 1930 is created by direct synthesis. The divide by 4 block 4802 creates a 231 MHz third LO (LO_3) consisting of I and Q signals required to mix the 275 MHz second IF 1922 down to the third and final IF frequency of 44 MHz 1926. A second down conversion to the 275 MHz third IF is used in the design. If a 1,200 MHz first IF signal were down converted directly to 44 MHz a local oscillator signal of 1156 MHz (1,200 MHz - 44 MHz) would be required. A resulting image frequency for this local oscillator would be at 1,112 MHz (1,200 MHz - 88 MHz). A 1,112 MHz image would fall within the band of the 1,200 MHz LC filter. Thus, there would be no rejection of this image frequency from the first IF's filter since it falls in the pass hand.

Therefore, the intermediate frequency conversion to a second IF of 275 MHz is used to reduce the effects of the problem.

The 231 MHz third LO 1936 falls close to the center of the received signal band width 1906. With the three frequency conversions of the design the third LO necessarily falls within the received signal band. This is undesirable from a design standpoint. This is because any spurious responses created by a third local oscillator signal fall within the received signal bandwidth. The present embodiment of this invention advantageously minimizes these undesirable effects.

In generating the third LO signal of 231 MHz, typically a phase lock loop containing a voltage controlled oscillator would be used. However, these frequency components tend to be primary generators of spurious products that tend to be problematic. The present embodiments of the invention advantageously avoids the use of a PLL and the attendant VCO in producing the third LO signal 1930 at 231 MHz. A divide by 4 circuit 4802 utilizes two flip-flops that create the I and Q third LO signals 1930 from the 925 MHz second LO 1904. This simple direct synthesis of the third LO tends to produce a clean signal. The reduced generation of distortion within the signal band tends to be important in an integrated circuit design where all components are in close physical proximity. If a PLL were used to generate the 231 MHz signal an external loop filter for the PLL would be utilized, providing another possible path for noise injection. By elegantly generating this third LO, that necessarily falls within the received signal bandwidth, noise and interference injection through the substrate into the received signal path tends to be minimized.

LC filter tuning 4812,4814,4816 in the embodiment is advantageously performed at startup of the chip. A "1,200 MHz filter tuning" circuit 4812 tunes the 1,200 MHz low pass filters 1912; a "275 MHz filter tuning" circuit 4814 tunes the 275 MHz

low pass filter 1934; and a "44/36 MHz filter tuning" circuit 4816 alternatively tunes a final LC filter 1936 to one of two possible third IF frequencies (44 MHz or 36 MHz) depending upon the application. Alternatively, in this embodiment, the filtering of the third IF frequencies is done by an external filter 4818. This external filter may have a saw device or other type of filter that provides satisfactory filtering of the third IF frequency.

In an embodiment an intermediate frequency automatic gain control amplifier ("IF AGC") 3419 is used to provide a nearly constant IF frequency signal level to IF signal processing/demodulating circuitry (3416 of FIG. 34).

Often the signal level variations being compensated for by the IF AGC are created by improperly tuned filters. The on chip filter tuning utilizing one or more existing PLL signals tends to reduce signal level variations.

As previously described, the filter tuning circuits 4812,4814,4816 utilize tuning signals based on the PLL2 signal 4806, with the "44/36 MHz filter tuning" circuit utilizing the PLL2 frequency divided by four 4802. However, the tuning signals selected may vary. Any or all of the PLLs 4804,4806,4802 or reference oscillator 4808 may be used to generate a filter tuning signal. Also a single frequency can be used to tune all filters with the appropriate frequency scaling applied. In tuning the LC filters, first the chip is turned on and PLL2 4806 must lock. PLL2 must first lock at 925 MHz as previously described. A VCO in the PLL 4806 is centered by adjusting its resonant circuit with tunable capacitors as previously described.

Once the PLL2 is adjusted to 925 MHz a write signal is sent out to indicate that a stable reference for filter tuning is available. Once a stable 925 MHz reference for tuning is available the 1,200 MHz filter, the 275 MHz filter tuning previously described takes place. Once the filter tuning is

finished the filter tuning circuitry sends out a signal over an internal control bus structure, linking the receiver to a controller indicating that the tuning has finished. The receiver is now ready to select and tune a channel.

Frequency tuning of received channels is accomplished in the embodiment with a coarse and fine PLL adjustment as previously described. The tuning is performed in such a way that there is always a third IF present at the output during the tuning process. PLL1 4804 is the coarse tuning PLL that tunes in 10 MHz steps. PLL2 4806 is the fine tuning PLL that tunes in 100 KHz steps. Exemplary tuning steps can be made as small as 25 KHz. A 100 kHz step is used for QAM modulation, and a 25 KHz step is used for NTSC modulation.

At the input of the tuner each exemplary channel is separated by 6 MHz. PLL1 jumps in tuning steps of 10 MHz. Therefore, + or - 4 MHz is the maximum tuning error. If the filters used had a narrow band pass characteristic this tuning approach tends to become less desirable. For example, if the filter bandwidth was one channel, 6 MHz, wide and the first IF could be 1204 MHz or 1196 MHz. Thus, the selected channel would not be tuned. The bandwidth of the cascaded filters in the first IF strip is approximately 260 MHz. The bandwidth of the filters centered at 275 MHz in the second IF strip is approximately 50 MHz. The bandwidths are set to be several channels wide, a characteristic that advantageously takes advantage of the low Q in the LC filters built on the chip. The two PLLs guarantee that a third IF output is always obtained. The first PLL that tunes coarsely must tune from 1,250 to 2,060 MHz, a wide bandwidth. PLL2, the fine tuning PLL, must tune from + to - 4 MHz, which tends to be easier to implement.

FIG. 51 shows a second exemplary embodiment of the invention. This embodiment is similar to the embodiment of FIG. 48, however it eliminates the first IR reject mixer (4802

of FIG. 48). The approximately 35 dB of image rejection that has been eliminated due to the removal of the IR reject mixer is made up by increased filter rejection provided by a 1,200 MHz LC filter bank 5101. The IR reject mixer is replaced with a conventional differential mixer 5104. The IO required is a single differential LO signal 5106 rather than the differential I and Q signals previously described. Better filters are used or alternatively an additional series of three 1,200 MHz LC filters 1912 for a total of six cascaded filters 5101 to provide sufficient image rejection are provided. This design provides the advantage of being simpler to implement on an integrated circuit.

If a higher Q or better filter selectivity is realized on the integrated circuit 65 dB of image frequency rejection at 650 MHz is required. In an alternate embodiment of the invention the third down conversion can be accomplished in a similar manner by eliminating the third I/Q mixer 4806 and increasing the selectivity of the 275 MHz filter bank 5102. The mixer 4806 is replaced with a conventional mixer requiring only a single differential third LO.

FIG. 52 shows a third alternate embodiment of the invention that tends to provide continuous tuning of the filter over temperature, and tends to more accurately keeps the response curve of the filter centered on the desired frequency. This embodiment of the invention preserves the separation of I 5202 and Q 5204 signals through the second IF stage 5206. In the third frequency conversion stage 5208 the I and Q signals are transformed into I′, $\bar{I}$, Q, and $\bar{Q}$ signals. This alternate embodiment of the invention relies on a "three-stage poly phase" 5210 to provide image cancellation. The advantage of using a gyrator in place of dual LC filter bank 5212 is that a close relationship between I and Q tends to be maintained throughout the circuit. The phase relationship at the output of the gyrator

filter tends to be very close to 90°. If an LC filter is utilized there is no cross-coupling to maintain the phase relationship as in the gyrator. In the LC filter configuration complete reliance upon phase and amplitude matching is relied upon to maintain the I and Q signal integrity. The gyrator circuit has the additional advantage of tending to improve the phase relationship of signals initially presented to it that are not exactly in quadrature phase. For example, an I signal that is initially presented to the gyrator that is 80° out of phase with its Q component has the phase relation continuously improved throughout the gyrator such that when the signals exit the gyrator quadrature phase of 90° tends to be established between the I and Q signals, such as in a polyphase circuit element. This present embodiment of the invention provides the additional benefit of being easily integrated onto a CMOS substrate since the gyrator eliminates the inductors that an LC filter would require. Filter timing and frequency generation utilize the methods previously described.

FIG. 53 is a block diagram of an exemplary CATV tuner that incorporates an embodiment of the present invention. The exemplary embodiments of the receiver are for terrestrial and cable television reception of signals from 50 to 860 MHz. Television signals in this exemplary band are frequency QAM or NTSC modulated signals. A receiver as described performs equally well in receiving digital or analog signals. However, it is to be understood that the receiver architecture disclosed will function equally well regardless of the frequencies used, the type of transmission, or the type of signal being transmitted. With regard to signal levels input to the receiver, the dynamic range of the devices used in the receiver may be adjusted accordingly. Thus, in a wide-band receiver distortion products are particularly problematic. The receiver disclosed in the exemplary embodiments of the present invention tends to

advantageously reduces interference problems created by this type of distortion.

In the exemplary embodiments of the invention signals input to the receiver may range from +10 to +15 dB_m. Where, zero dB_m = 10 log(1 mV/1 mV). It should be noted that in the case of a cable transmitting the RF signals, that an attenuation envelope impressed on the signals will have a downward or negative slope. This downward or negative slope is a result of a low pass filter characteristic of the coaxial cable. This effect may be compensated for by introducing a gain element in the signal chain that has positive slope, to compensate for the negative slope resulting from cable transmission.

In a wide band receiver designed to process signals received over multiple octaves of band width, this transmission characteristic can present a problem. For example, in the cable television band going from 50 to 860 MHz it is possible for distortion products created by the lower frequency signals in this band width to fall upon one of the higher tuned frequencies, for example 860 MHz. In a multi octave band-width receiver harmonic signals are problematic since they also fall within the receiver band-width, and cannot be low pass filtered out. If a channel at one of the higher frequencies is the desired signal that the receiver is tuned to, the low pass filter characteristic of the cable, or transmission medium, reduces the strength of this desired tuned signal relative to the lower frequency untuned signals. Because of the relatively greater strength of the lower frequency signal, the strength of the distortion products generated by them, are comparable in strength to the desired tuned signal. Thus, these distortion products can cause a great deal of interference with the desired received signal when one of their harmonics coincidentally occurs at the same frequency as the tuned signal.

The frequency plan of this tuner allows it to be implemented in a single CMOS integrated circuit 4822 and functions as previously described in FIG. 48. This exemplary single up-conversion dual down conversion CATV tuner utilizes two PLLs that run off of a common 10 MHz crystal oscillator 5302. From the 10 MHz crystal oscillator references the PLLs generate two local oscillator signals that are used to mix down a received radio frequency to an intermediate frequency. This integrated CATV tuner advantageously uses differential signals throughout its architecture to achieve superior noise rejection and reduced phase noise. The receiver of the present invention advantageously provides channel selectivity and image rejection on the chip to minimize the noise injected into the received signal path. The differential configuration also tends to suppress noise generated on the CMOS substrate as well as external noise that is radiated into the differential leads of the 10 MHz crystal that connect it to the substrate. In this embodiment, an external front end as previously described is supplied on a separate chip 5304 and an external filter 5306 is utilized.

The details of integrated tuners are disclosed in more detail in U.S. Patent Application No. 09/439,101 filed November 12, 1999 (B600:33756) entitled "Fully Integrated Tuner Architecture" by Pieter Vorenkamp, Klaas Bult, Frank Carr, Christopher M. Ward, Ralph Duncan, Tom W. Kwan, James Y.C. Chang and Haideh Khorramabadi; based on U.S. Provisional Application No. 60/108,459 filed November 12, 1998 (B600:33586), the subject matter of which is incorporated in this application in its entirety by reference.

TELEPHONY OVER CABLE EMBODIMENT

FIG.54 is a block diagram of a low power embodiment of the receiver that has been configured to receive cable telephony

signals. These services among other cable services offered make use of RF receivers. A cable telephone receiver converts an RF signals present on the cable to a baseband signal suitable for processing to an audio, or other type of signal routed to a telephone system and a subscriber via two way transmission. When such services are widely offered, and are packaged into a common device, per unit cost and power dissipation tend to become concerns. It is desirable to provide a low cost and power efficient receiver.

Receivers integrated onto a single chip that incorporates filters on the chip reduce cost. However, placing filters onto a an integrated circuit results in a high power consumption by the chip. On chip filters require tuning circuitry that tends to consume significant amounts of power. Removal of this circuitry allows reduction of power levels to below 2 Watts per receiver. Each time that a signal is routed off of an integrated circuit the chances of increasing system noise are increased due to the susceptibility of the external connections to the pick up of noise. Careful signal routing and the proper frequency planning of the present embodiment are calculated to reduce these undesired effects.

First, an input signal is passed through an RF front end chip 5304 as previously described. The first frequency up conversion to the first IF 5402 is performed on the integrated receiver chip. After passing a 50-860 MHz signal through a receiver front end 5304 that provides a differential output to the receiver chip 5404 the signal is down converted to 1,220 MHz 5402. The 1,270 to 2,080 MHz LO 5406 is generated on chip by a first PLL circuit, PLL1 5408. The 1220 MHz differential signal is passed through buffer amplifiers 5410 and is applied to an off chip differential signal filter 5412, with a center frequency at 1,220 MHz having a characteristic impedance of 200 Ohms. The differential signal tends to provide the necessary noise

rejection when routing the signal off and subsequently back onto the chip. Next the signal is routed back on to the integrated circuit 5404 where it is again passed through a send buffer amplifier 5414.

The second frequency down conversion to the second IF 5416 is performed on the integrated receiver chip. An 1,176 MHz differential I and Q LO 5418 is generated on the integrated circuit by a second PLL, PLL2 5420 and polyphase 5422. The resulting second IF frequency 5616 is 44 MHz. The mixer used to generate the second IF is an I/Q type mixer 5424 that subsequently passes the signal through a polyphase circuit 5426. The second IF is then passed through a third buffer amplifier 5428. The signal is next routed off chip to a differential filter centered at 44 MHz 5430. After filtering the signal is returned to the integrated circuit where it undergoes amplification by a variable gain amplifier 5432.

Variable gain amplifier ("VGA") 5432 utilizes cross coupled differential pairs as described in FIG. 74. The improved dynamic range of the VGA compensates for increased variations in signal amplitude caused by irregularities in the external differential filter 5430. By operating satisfactorily over a wide dynamic range of input signal levels the filter requirements may be relaxed, allowing for a more economical receiver to be constructed.

The details of a low power receiver design are disclosed in more detail in U.S. Patent Application No. 09/439,102 filed November 12, 1999 (B600:36232) entitled "System and Method for Providing a Low Power Receiver Design" by Frank Carr and Pieter Vorenkamp; based on U.S. Provisional Application No. 60/159,726 filed October 15, 1999 (B600:34672), the subject of which is incorporated in this application in its entirety by reference.

ELECTRONIC CIRCUITS INCORPORATING EMBODIMENTS OF THE RECEIVER

FIG. 55 shows a set top box 5502 used in receiving cable television (CATV) signals. These boxes typically incorporate a receiver 5504 and a descrambling unit 5506 to allow the subscriber to receive premium programming. Additionally, on a pay for view basis subscribers can order programming through their set top boxes. This function additionally requires modulation circuitry and a radio frequency transmitter to transmit the signal over the CATV network 5508.

Set top boxes can, depending on the nature of the network, provide other services as well. These devices include, IP telephones, digital set-top cards that fit into PCs, modems that hook up to PCs, Internet TVs, and video conferencing systems.

The set-top box is the device that interfaces subscribers with the network and lets them execute the applications that reside on the network. Other devices in the home that may eventually connect with the network include IP telephones, digital set-top cards that fit into PCs, modems that hook up to PCs, Internet TVs, and video conferencing systems.

To satisfactorily provide digital services requiring high bandwidth, set top boxes must provide a easy to use interface between the user and CATV provider. Memory 5510 and graphics driven by a CPU 5512 tend to make the application as appealing as possible to a user when interfaced with a set top box 5514.

Also the set-top can receive data in Internet Protocol format and has an IP address assigned to it. Also, satisfactory methods of handling reverse path communications are required to provide interactive digital services. All of these services utilize an operating system resident in the set top box 5502 for providing a user interface and communicating with the head end 5514 where the services are provided.

To receive services, and transmit requests for service, bidirectionally across a CATV network the data signal must be

modulated on a RF carrier signal. The set top box is a convenient place to modulate the carrier for transmission, or to convert the modulated carrier to a base band signal for use at the user's location.

This is accomplished with a radio frequency (RF) transmitter and receiver, commonly referred to in combination as a transceiver 5508. A bidirectional signal from a cable head end 5514 is transmitted over a cable network that comprises cable and wireless data transmission. At the subscriber's location a signal 3406 is received an input to the subscriber's set top box 5502. The signal 3406 is input to a set top box transceiver 5504. The set top box transceiver 5504 comprises one or more receiver and transmitter circuits. The receiver circuits utilized are constructed according to an embodiment of the invention. From the set top box transceiver, received data is passed to a decryption box 5506. If the television signal has been encrypted, this box performs a necessary descrambling operation on the signal. After being passed through the decryption box, the signal next is presented to a set top box decoder 3416 where the signal is demodulated into audio and video outputs 3414. The set top box incorporates a CPU 5512 with graphics capabilities and a memory 5510 to provide an interface and control the set top box through a data transfer structure 5514. An optional input output capability 5516 is provided for a direct user interface with the set top box. To transmit instructions from the user to the head end, information is transmitted over data transfer structure 5514 into the transceiver module to the internal transmitter via the cable TV network to the head end.

FIG. 56 is an illustration of the integrated television receiver 5602. This television could be one that processes digital or analog broadcast signals 5604. An exemplary integrated switchless attenuator and low noise amplifier 3408

is the first stage in a receiver contained in a television set. The integrated switchless attenuator and low noise amplifier is used as a "front end" of the receiver to adjust the amplitude of the incoming signal. Incoming television signals whether received from a cable or antenna vary widely in strength, from received channel to channel. Differences in signal strength are due to losses in the transmission path, distance from the transmitter, or head end, obstructions in the signal path, among others.

The front end adjusts the received signal level to an optimum value. A signal that is too strong produces distortion in the subsequent circuitry by over driving it into a non linear operating region. A signal that is too week will be lost in the noise floor when subsequent high noise figure circuitry is used in an attempt to boost the signal strength. When used in conjunction with "automatic level control" (5604) circuitry the integrated switchless attenuator and low noise amplifier responds to a generated feed back signal input to its control voltage terminal to adjust the input signal level to provide optimum performance.

After passing through the front end 3408, the RF signals 5604 are input to tuner 5620. This tuner circuit is as described in the previous embodiments where a single channel is selected from a variety of channels presented in the input signal 5604. An automatic fine tuning circuit ("AFT") 4622 is provided to adjust the level of the final IF signal 5624 being output to the television signal processing circuitry 5610. The signal processing circuitry splits the audio signal 5602 off of the final IF signal 5624 and outputs it to an audio output circuit such as an amplifier and then to a speaker 5618. The video signal split from IF signal 5624 is delivered via video signal 5606 to video processing circuitry 5612. Here the analog or digital video signal is processed for application as control

signals to the circuitry 5614 that controls the generation of an image on a display device 5626. Such a receiver would typically be contained in a television set, a set top box, a VCR, a cable modem, or any kind of tuner arrangement.

FIG. 57 is a block diagram of a VCR that incorporates an integrated receiver embodiment 5702 in its circuitry. VCRs are manufactured with connections that allow reception and conversion of a television broadcast signal 5704 to a video signal 5706. The broadcast signals are demodulated 5708 in the VCR and recorded 5710 on a recording media such as a tape, or output as a video signal directly. VCRs are a commodity item. Cost pressures require economical high performance circuitry for these units to provide additional more features as the prices decline in the marketplace.

FIG. 58 shows a block diagram of a typical cable modem. A "Cable Modem" is a device that allows high speed data connection (such as to the Internet) via a cable TV (CATV) network 5812. A cable modem commonly has two connections, one to the cable TV wall outlet 5802 and the other to a computer 5804.

There are several methods for connecting cable modems to computers, Ethernet 10BaseT is an example. The coax cable 5808 connects to the cable modem 5806, which in turn connects to an Ethernet card 5814 in a PC. The function of the cable modem is to connect broadband (i.e., the cable television network) to Ethernet. Once the Ethernet card has been installed, the TCP/IP software is typically used to manage the connection.

On-line access through cable modems allows PC users to download information at a speeds approximately 1,000 times faster than with telephone modems. Cable modem speeds range from 500Kbps to 10Mbps. Typically, a cable modem sends and receives data in two slightly different, or asynchronous fashions.

Data transmitted downstream, to the user, is digital data modulated onto a typical 6 MHz channel on a television carrier,

between 42 MHz and 750 MHz. Two possible modulation techniques are QPSK (allowing data transmission of up to 10 Mbps) and QAM64 (allowing data transmission of up to 36 Mbps). The data signal can be placed in a 6MHz channel adjacent to an existing TV signals without disturbing the cable television video signals.

The upstream channel to the ISP provider is transmitted at a rate between 5 and 40 MHz. This transmission path tends to inject more noise than the downstream path. Due to this problem, QPSK or a similar modulation scheme in the upstream direction is desirable due to noise immunity above that available in other modulation schemes. However, QPSK is "slower" than QAM.

Cable modems can be configured to incorporate many desirable features in addition to high speed. Cable modems can be configured to include, but are not limited to, a modem, a tuner 5816, an encryption/decryption device, a bridge, a router, a NIC card, SNMP agent, and an Ethernet hub.

To transmit and receive the data onto the cable television channel it must be modulated and demodulated respectively. This is accomplished with a radio frequency (RF) transmitter and receiver, commonly referred to in combination as a transceiver 5818. The receiver's front end 5820 is advantageously provided as previously described.

ESD PROTECTION

FIG. 59 is an illustration of a typical integrated circuit die layout. An IC die 5900 is typically laid out with a series of pads 5904 at the edge of the die. This peripheral area of the die is referred to as the pad ring 5906. Typically at the center of the die a core 5902 is located. The core contains the circuit functions being performed on the integrated circuit die 5900. An integrated circuit die is typically placed inside of an IC package or "header". The IC package provides a mechanically sturdy package to protect the die 5900 and interface reliably

with external circuitry. The pads 5904 in the pad ring 5906 are typically wire bonded to pins fixed in the header. Arranging pads 5904 in a peripheral pad ring 5906 allows for ease in an automated wire bonding from header pins to the pads of the die 5900.

Thus, on an IC die 5900, typically configured as shown in FIG. 59, the pads 5904 located in the pad ring 5906 are an intermediate connection between the circuit core 5902 and outside connections on the IC package.

The pad ring of an integrated circuit die typically provides a convenient place to provide electrostatic discharge ("ESD") protection circuitry. ESD discharge occurs when static build-up of electrical charge occurs. A static charge build-up typically comprises a high voltage until discharged. A static charge built up upon a surface will jump, or arc, to another surface of lower potential once the voltage difference between the surfaces exceeds a spark gap voltage for a dielectric, that separates the two surfaces. Spark gap voltages are typically rated in volts per inch. This is the voltage required to arc from one surface to another, located one inch away from each other with a given material present between the surfaces. For a given separating material a charge will arc from one surface to the other for a lower value of potential if the surfaces are moved closer together. In integrated circuits distances between conductors or devices present on an integrated circuit tend to decrease as the degree of miniaturization increases. Thus, electrostatic discharge from one surface to another within an integrated circuit tends to occur at smaller voltages as the state of the art advances.

ESD is a major source of integrated circuit damage. After a charge builds up to a point where it arcs from one surface to another, the arcing causes damage to the integrated circuit.

Typical damage comprises holes punched in a substrate and destruction of transistors in the core 5902.

ESD protection is typically provided by a device that provides a low impedance discharge path from an IC pin to all other pins including ground when an ESD charge exceeds a predesigned threshold voltage of the protection device. During normal operation of the circuit the ESD device does not cause a loading at the IC pin. Better ESD protection tends to be produced when a lower trigger threshold is provided in the ESD protection circuit. (ESD circuits provide a low impedance discharge path from any pin of an integrated circuit to any other pin once an ESD triggers a given threshold designed into an ESD circuit). Thus, to protect integrated circuits from ESD signal isolation from pin to pin is undesirable. To withstand an ESD event, large structures with sufficient spacing tend to provide increased ESD protection.

However, from a signal isolation prospective, it is desirable to have a high signal isolation between integrated circuits pins. Isolation between pins is particularly desirable in RF integrated circuits. To function properly, circuits tend to require power supply lines, ground lines and signal lines that are isolated. ESD circuitry conflictingly tends to require all pins to be interconnected somehow. Furthermore, RF IC's tend to need small structures in order to enhance bandwidth and reduce noise. This requirement is contradictory to an ESD's circuits requirement for structures that handle large currents.

An increasing trend in integrated circuit design is to mix high speed and/or high frequency circuitry with high digital circuits. Digital circuits tend to generate high noise levels within an IC. Digital circuit noise tends to interfere with other circuit functions present on the die. The individual circuits present on the die are often designed in blocks that define a given area on the die substrate. These circuit blocks

containing sensitive circuitry are shielded as much as possible from the digital circuitry.

A common technique to minimize noise injection is to put different circuit blocks on separate power and ground lines. Sensitive circuits in this arrangement are placed as far as possible from noisy circuitry. While this arrangement tends to improve power supply and ground isolation, ESD discharge problems tend to be aggravated.

During ESD discharge a current flows from one to point to another through path of least resistance. If a path is not present, or inadequate, parasitic discharge paths tend to form causing damage to the integrated circuit. Thus, circuitry separated by large distances to minimize cross talk and noise injection tend to be susceptible to damage from ESD discharge over parasitic paths.

For example, for a noise sensitive mixed mode IC fabricated by a CMOS technology, a non-epitaxial process is preferred due to the processes ability to provide a higher substrate isolation. However, the non-epitaxial CMOS process tends to create undesirable ESD discharge paths due to a triggering of a parasitic bipolar structure inherent with the process. These discharge paths tend to pass through and damage core circuitry. Thus, it is desirable to provide a structure that tends to control ESD discharge paths.

From an ESD design standpoint, large ESD structures provide better protection than a smaller structure. However, in noise sensitive circuits, the large ESD structures connected to the circuitry tend to act as noise sources, degrading circuit performance. Thus insertion of ESD structures in noise sensitive circuits must be done with care.

FIG. 60 illustrates an embodiment of the invention that utilizes pad ring power and ground busses. A pad ring buss utilizes a reference VDD 6002 and a reference ground ring 6004

that run through the entire pad ring of a die along the exterior edge of the die. In an embodiment, the pads 5904 along an edge of the die are arranged in line. In an alternate embodiment, the pads 5904 may be staggered along the edge of the die 5900.

The reference VDD rings and reference ground rings serve to connect a series of localized power domains contained in the core 5902 of the die. Because of the block structure making up individual circuit functions within the core comprise localized power domains they connect to a primary power bus in the pad rings. The pad rings 6002, 6004 may be broken 6006 to prevent the formation of a current loop causing eddy currents. The pad rings are connected to individual power domains within the circuit through ESD discharge protection structures.

FIG. 61 is an illustration of the connection of a series of power domains 6102, 6104, 6106 to a pad ring bus structure 6002, 6004. On die 5900 pad rings 6002, 6004 are disposed about the periphery of an integrated circuit. The pad rings are provided with a gap 6006. The pad rings surround an integrated circuit core 5902 that comprises one or more circuit blocks 6102, 6104, 6106. Within each block a localized power and ground bus structure is provided for each block 6110, 6112, 6114 respectively. ESD discharge protection devices 6108 are utilized to prevent electrostatic discharge damage.

The localized bus structures 6110, 6112, 6114 are connected through ESD discharge protection devices to the pad rings at a single point. In this structure, no localized power supply or ground line is more than two ESD structures away in potential drop from any other voltage or ground structure.

FIG. 62 is an illustration of an embodiment utilizing an ESD ground ring 6200. In the embodiment shown a set of localized power and ground buses 6110, 6112, 6114 are located in a corresponding circuit function blocks 6102, 6104, 6106. It is understood that the localized power and ground busses may

contain multiple power and ground lines, and that for simplicity in explanation a single power supply line and ground line will be discussed. It is also understood that any number of circuit function blocks may be utilized in the circuit to provide the desired protection. The circuit function blocks are protected from ESD by utilizing the ESD ground ring 6200 coupled to a series of ESD protection devices 6204, 6108.

Each of the localized power and ground busses being protected is configured as in circuit function block 6102. The interconnections in circuit block 6102 will be discussed as a representative example of all connections. A discharge path for power supply lines is through the ESD protection device 6108 coupled between a local power line VDD1 and a local ground line GND1. The ESD ground ring and ESD protection devices provide isolation between the voltage buss and ground within the circuit blocks 6102, 6104, 6106. The structure also provides an ESD discharge path between any voltage bus line contained in another circuit function block and ground.

Local grounds 6110, 6112, 6114 are coupled through an ESD clamp structure 6204 to the ESD ground ring. To prevent eddy currents from forming, a gap 6006 is cut in the ESD ground ring 6200. A bond pad 6202 coupled to the ESD ground 6200 is provided to couple the ESD ground to a system ground. Coupling an ESD ground to a system ground tends to decrease noise that tends to be coupled through the ESD ground ring into the circuit core 5902.

In each circuit function block all individual grounds Gnd1 Gnd2 Gnd3 are connected to the ESD ground ring through a pair of anti-parallel diodes 6204. In addition to anti parallel diodes other ESD triggered protection devices may be equivalently utilized. Thus, with the connection described, any ground in any circuit block is only two diode potential drops (approximately

0.6 of a volt for a silicon diode) away from any other ground in any circuit block.

When implemented in a CMOS technology the substrate is conductive. In CMOS technology the ground lines in each block are inherently coupled to each other through the substrate. By going through the ESD ground ring the localized grounds tend to be loosely coupled to each other through the pair of anti-parallel diodes. Because of loose coupling between the substrate and ESD ground ring, noise coupling between the various grounds tends to be minimized.

The VDD lines in each block are completely isolated from each other. The ESD clamps 6108 between the VDD and ground lines in the circuit block tend to provide a complete discharge path for the VDD bus lines. When an ESD event occurs the VDD supply lines in a block sees a low impedance path through two diodes and two ESD clamps to the VDD bus of another circuit block.

RF and high speed signals present unique problems to providing ESD protection. Noise is typically injected in a circuit through the circuit's power supply and ground leads. Good high impedance RF isolation of noise sources from an RF signal while providing a low impedance ESD discharge path is provided by circuitry comprising an ESD pad ring. The embodiments tend to provide isolation of RF signals from noise sources by high impedance paths between the noise signal and RF signal while maintaining a low impedance discharge path from pin to pin of the integrated circuit when presented with an ESD signal. Thus, the dual requirement of an RF signal's need for isolation and an ESD circuit's needs for all pins to be connected tends to be achieved in the embodiments described above.

Another conflicting requirement is an RF circuit's need to maintain small structures that reduce noise coupling and enhance bandwidth by reducing parasitic capacitance verses an ESD

circuit's requirements for a large structure that will withstand a large ESD discharge current.

FIG. 63 is an illustration of the effect of parasitic circuit elements on an RF input signal. Parasitic effects tend to be more pronounced in a circuit structure with large physical dimensions such as a bonding pad. In a typical RF integrated circuit a bonding pad tends to have dimensions much greater than the circuit elements present on the integrated circuit. In addition bonding pads are attached to pins of an integrated circuit often by wire bonds that increase the parasitic effects. Parasitic elements tend to produce the affects of a low pass filter 6300. For simplicity the low pass filter is shown as a series resistor 6302 with a shunt capacitance 6304. However in an actual circuit it is understood that this resistance and capacitance comprises distributed elements disposed along the length of the bond wire and pad structure.

If an RF signal 6306 having a given bandwidth is presented to such a filtering structure 6300, then the signal emerging at the other end is a band limited or filtered signal 6308. Such a distorted signal is undesirable. In the case of an analog RF input signal information, or the signal its self may be lost. In the case of a digital signal, limiting the bandwidth of the spectral components that make up the pulse train causes distortion in the pulse train at the output. The capacitance 6304 tends to be produced predominantly by a bonding pad structure that separates the charge collected on the bonding pad from a ground underneath it.

In an ESD protection circuit large bonding pads and large ESD structures are desirable to shunt large ESD currents to ground without damage to the circuitry. However, when such a large ESD structure or bonding pad is present RF signals tend to be degraded due to the parasitic effects. Large capacitance is desirable from an ESD design standpoint. Large capacitors tend

to slow down a buildup of charge, and thus potential during an ESD event.

In addition cross-talk is produced by a signal on one line being capacitively coupled to a signal on a second line distance between the lines must be maintained. A reference ring routed about the periphery of a chip with bonding pads placed on the core side tends to reduce or eliminate the cross-talk that would occur between these conductors if one were routed on top of the other.

Returning to FIG. 59, in the state of the art power buses are typically disposed between the integrated circuit core 5902 and the pad ring 5906, with the bonding pads 5904 disposed about the periphery of the chip 5900. In this arrangement a pad to core connection typically crosses the power buses perpendicularly.

FIG. 64 illustrates a cross-talk coupling mechanism. A bonding pad 5904 disposed on the periphery of the die 5900 would require interconnecting traces 6404 to pass over ESD voltage and ground reference pad rings 6002, 6004. Any signal present on the integrated circuit track 6404 crossing over the ESD protection rings 6002, 6004 are capacitively coupled 6402. Signals on reference rings 6002 and 6004 will tend to be coupled onto trace 6404 and vice versa. Thus, it is desirable to place the bond pad 5904 within the periphery of the reference rings.

In an embodiment bond pads 5904 are disposed within the pad rings 6002, 6004. External connections are achieved with bond wire connections that cross over the pad rings. The crossover gap of the bond wire is much larger than the vertical distance between the circuit track 6404 and either of the reference rings 6002, 6004.

FIG. 65 is an illustration of an ESD device disposed between a connection to a bonding pad and power supply traces. In a typical IC layout a bonding pad 5904 is connected 6404 to an

integrated circuit core 5902. Traces 6504 typically cross power supply and ground lines 6002 6004. An ESD device 6500 is typically disposed between the traces and the power supply buses. A parasitic capacitance exists between the traces 6404 and the power supply connections 6002, 6004. This parasitic capacitance reduces signal bandwidth and degrades noise performance because of the low pass filtering affect. Also, with this arrangement a core circuit 5902 must be distanced from the bonding pad 5904 to allow for the power supply traces 6002, 6004 to pass between the pad and core. This prevents minimization of the distance between bonding pad and circuit core. Parasitic capacitance between power supply conductors and traces connecting the core to the bonding pad are not the only problem encountered with this configuration. In the current state of the art the bonding pads tend to increase parasitic capacitance.

FIG. 66 is an illustration of parasitic capacitance in a typical bonding pad arrangement on an integrated circuit. In a typical integrated circuit a large bonding pad is disposed on the surface of the integrated circuit die 5900. To prevent pad peeling and liftoff one or more metal layers 6600 are disposed in a layered structure separated by semiconductor material or oxide. The two metal layers 6602, 6604 shown are coupled to the upper metal layer 5904 by multiple feed-throughs 6606 that provide electrical contact and mechanical stability to the uppermost bond pad 5904. With this structure multiple parasitic capacitance 6610 due to the layout are present. These parasitic capacitances will couple to the substrate or any circuit traces disposed nearby such as a power and ground bus structure.

FIG. 67 is an illustration of a embodiment of a bonding pad arrangement tending to reduce parasitic capacitances. A pad ring bus comprised of lines 6002, 6004, 6200 is disposed about the periphery of the chip 5900. ESD devices 6702 are disposed to the side of a bonding pad 6704. With this arrangement a bonding pad

6704 may be connected 6504 to a circuit block in the core 5902 with a minimum interconnecting trace length. The pad to core connection 6504 does not overlap any power ground or ESD bus structure. Thus, cross-talk and noise coupling with these structures tends to be minimized. In addition the metal routing width from core to bonding pad is not restricted due to requirements that would be imposed by an ESD structure as described in FIG. 67. In an alternate embodiment that provides improved ESD handling capabilities, the ESD structures 6702 may be increased in size.

In an alternative embodiment the ESD ground bus 6200 is placed at the periphery of the die. This bus tends to carry noise that is most disruptive to circuit operation. Thus, it is desirable to space this bus as far as possible from a pad. In the alternate embodiment the ground bus is disposed between the ESD ground bus and the VDD bus to reduce coupling between the ESD ground bus and the VDD bus line.

FIG. 68 illustrates a cross section of the bonding pad structure of FIG. 67. The bond pad 5904 is reduced in size to the smallest dimension allowable for successful product manufacturing. A second metal layer 6802, further reduced in area as compared to the top layer, is utilized as an anchor to hold the bonding pad above it in place during a bonding process. With this arrangement a smaller number of feed-through connections 6606 are required. By eliminating multiple metal layers beneath the top layer 5904 a distance between the lower bond pad 6802 and the substrate 5900 is increased. As predicted from the capacitance formula, when the distance is increased

between capacitor plates the parasitic capacitance is decreased. The relationship is as follows:

$$C = K\varepsilon r \times (A/d) \qquad (13)$$

where

C = capacitance
K = dielectric constant
εr = the relative dielectric constant of the separating material
A = area of the conducting plates
d = distance between the conducting plates

As can also be seen from the equation the reduced area of the bonding pad results in a smaller capacitance. In addition, if the dielectric constant in the equation is lowered then the capacitance will also be lowered.

A diffusion area 6804 is disposed beneath the bonding pads 5904,6802 to decrease the capacitance from bonding pad to substrate. The diffusion area comprises a salicided diffusion implant 6804 to further reduce parasitic capacitance coupling to the substrate. This diffusion area 6804 is coupled to a potential 6806 that tends to reduce a voltage difference between the diffusion layer 6804 and the bond pad structure 5904, 6802.

FIGS. 69a-69e illustrate various ESD protection schemes utilized in the state of the art to protect an integrated circuit from ESD discharge due to charge build up on a die pad. Typically a large ESD structure (or clamping device) attached to an IO pin of a CMOS integrated circuit allows a high ESD discharge current to be shunted to ground through it. However, a large ESD structure on an IO pin causes two problems. First dedicating a large area on an integrated circuit die to an ESD structure is undesirable. Die size is directly related to the cost of manufacturing making a minimized die size desirable. A

second problem with a large ESD structure is a capacitive loading by the ESD structure on a signal present on the pin. The loading causes a decrease in bandwidth of the input signal, increased power dissipation, and exceeding the allowable specified input capacitance. A compact ESD protection structure that works in conjunction with over-voltage protection, has a fast response time, will not be turned on by noise generated in normal operation, and provides a layout that may be used by multiple semiconductor foundries is described in the following paragraphs.

In the past various structures 6902, 6904, 6906, 6908, 6910 have been coupled to IC die pads 5904 to shunt away harmful ESD levels. A common structure is the ggNMOS ESD structure 6902. A ggNMOS transistor M1 is utilized to shunt an ESD charge to ground. The source of M1 is tied to the pad, and the drain to ground. Equivalently the drain may be tied to a lower potential source. As ESD charge builds on the pad its voltage increases to a point where the ggNMOS transistor is triggered to conduct the ESD charge to ground.

Internal capacitance in the ggNMOS transistor feeds a portion of the voltage established by a static charge to the ggNMOS transistor gate. When the voltage has risen to a sufficient level on the gate the transistor conducts. When conducting the transistor is in a low impedance state and all the static charge on the pad is shunted to ground.

Until the gate voltage rises to a level to cause the transistor to conduct it is in an off, or high impedance state. In this state the ggNMOS transistor tends to not disturb the signal on the pad.

Gate bias determines the effectiveness of this structure. In normal operation the gate of the ggNMOS is biased off putting the NMOS in an off, or high impedance state. Under an ESD discharge condition the gate of the ggNMOS is biased high to turn on a channel under the gate oxide. The ggNMOS relies on the

transistor's inherent capacitance from gate to drain ("Cgd") to pull the gate high when the pad is pulled high when a large electrostatic charge is present. Triggering is set by a voltage divider circuit comprising Cgd and resistor R. The electrostatic charge on the pad 5904 is divided down by the ratio of impedances of the capacitor Cgd and resistor R.

Coupling through Cgd degrades in a typical cascode over-voltage protection circuit. The ggNMOS cannot be used alone without a series cascode transistor 6904 when its voltage from drain to source ("VDS") exceeds a given electrical overstress limit. The ggNMOS M1 utilizes a series cascode stage M5, with its gate biased on, as shown at 6904 prevents Cgd from being directly coupled to a bonding pad 5904, substantially impairing its effectiveness. To circumvent insufficient coupling of M1's Cgd to the pad three other device configurations 6906, 6908, 6910 are known.

The first device 6906 adds capacitor C1 to the ggNMOS structure of 6902. C1 is coupled from gate to source of M1. C1 increases the coupling effect produced by the inherent Cgd of the ggNMOS. Unfortunately C1 strongly couples the ggNMOS to the pad. Slight perturbations present on the pad during normal operation are directly coupled to the ggNMOS through the strong coupling. Thus, with the added coupling capacitor C1 present, typical AC noise present on the pad tends to turn on the ggNMOS during normal operation.

The next circuit 6908 utilizes the same coupling capacitor C1 as described in 6906. However, this coupling capacitor has one terminal tied to the gate of M1 and the second terminal tied to a power supply voltage. During an ESD event the power supply is pulled high by the ESD voltage present on the pad. When the power supply is pulled high the gate of the ggNMOS M1 follows it to a high state. However with this arrangement the gate of the ggNMOS is directly coupled to a noise typically present on a

power supply line. Switching noise present on a power supply line tends to cause the ggNMOS M1 to turn on. If a quiet, or filtered, power supply is coupled to capacitor C1 an extra voltage drop caused by going through ESD protections of the quiet power supply would be required before the gate bias is pulled high. This causes an undesirably slow response time.

The third method 6910 utilizes a zener diode Z1 connected with the positive terminal at the gate of M1 and its negative terminal to the source of M1 to pull the gate of the ggNMOS high under an ESD discharge. When an ESD discharge event occurs the zener diode goes into a voltage breakdown mode allowing charge to flow to the gate of the ggNMOS M1. The gate floats high and the ggNMOS turns on shunting the ESD current to ground. The drawback of this approach is that zener diodes are not available in standard digital CMOS process.

FIG. 70 illustrates an approach to pad protection during ESD event. Electrostatic charge builds up on an integrated circuit pad 5904. A shunt device 7002 is connected from the pin 5904 to ground. The shunt device 7002 is in a high impedance state until sufficient charge builds up upon the pad 5904 to trigger the shunt device into a low impedance state. A low impedance state allows all of the charge built up upon the pad to be shunted to ground before damage to circuitry coupled to the pad can occur. The shunt device is triggered by the ESD charge building on the pad. A divider circuit comprising a capacitive element 7006 in series with a resistive element 7004 are coupled between the pad 5904 and ground. The junction of the capacitive and resistive element is used as a trigger to the shunt device 7002. When a preset trigger voltage is reached the shunt device is activated into a low impedance state.

FIG. 71 is a schematic of a circuit immune to noise that uses an ggNMOS' Cgd and a gate boosting structure to trigger ESD protection. In this configuration diode CR1, transistors M2 and

M3 are all disposed in an n-well biased at a voltage V to form a gate boosting structure 7102. The source and drain of M3 are coupled to the n-well 710. The source of transistor M2 is tied to a quiet power supply V. Power supply V is used to provide back gate bias in the N-well. CR1 is made by a P+ diffusion into the n-well. Typically only one quiet power supply is sufficient to bias the entire chip. This is because CR1 is fabricated with small dimensions and dissipates little power.

Transistor M3 is a PMOS transistor operating in its linear region to provide a MOS capacitor inherent to its construction between CR1 and R1. The drain of M2 is coupled to the source of M3. The drain of M3 is coupled to the negative terminal of CR1. The positive terminal CR1 is coupled to the pad 5904. The gate of M3 is coupled to a first terminal of resistor R1, and a second terminal of R1 is coupled to ground. The junction of the gate of M3 and R1 is tied to the gate of M1 and the negative terminal of CR1. The drain of M1 is tied to pin 5904 and the source of M1 is tied to ground. Alternatively the ground connection is not at zero potential but some lower potential. Resistor R1 is fabricated as an ohmic resistor, or alternatively using other pulldown techniques known in the art.

In normal operation M2 is turned on. This provides a low impedance path from the n-well back gate 7100 which is the n-well that host 7102 to the quiet power supply V. The channel side, that is formed by the gate and conductive channel formed in the silicon between the source and drain, of the MOS capacitor formed by M3 is thus tied to a low impedance source. Diode D1 is reverse biased forming a high impedance path between M3 and pad 5904. Thus, a strong coupling between the MOS capacitor formed by M3 and the pad is not present. Added input capacitance tends to be negligible by keeping the dimensions of diode CR1 as small as allowed by a process' constraints.

When electrostatic discharge occurs CR1 becomes forward biased, providing a low impedance path from the pad 5904 to the capacitor formed by M3. In response the capacitor formed by M3 charges up, providing a "boosting" to turn on the gate of M1. By providing boosting to the gate of M1 the drain source channel in M1 is turned on quickly forming a low impedance connection from the pad 5904 to ground. The fast response time is particularly suitable for a machine model ("MM") and charge device model ("CDM") ESD discharge modes.

The MOS capacitor formed by M3 significantly increases the capacitance present on the gate of M1. This allows R1 to be reduced in size to maintain the same time constant τ ($\tau=1/R\times C$) that would otherwise be required if M3 were absent. Without the presence of the capacitance of M3, R1 would be required to be in the range of hundreds of kilo-Ohms. Resistors of this value require a large amount of layout area.

Thus R1 and CR1 do not require significant die area. The fabrication of M3 utilizes thin oxide to form the MOS capacitor also providing a compact layout of this device. M1 is also reduced in size because of the gate boosting provided. In the configuration described, M1 is biased at a higher gate source voltage allowing a channel to conduct current more efficiently. Thus, a given ESD current is capable of being conducted to ground with a smaller transistor M1. The dimensions of M1 do not need to be made large in order to provide sufficient Cgd for gate boosting, since boosting is primarily accomplished through the capacitance supplied by M3.

FIG. 72 is a schematic of an alternative embodiment utilizing the gate boosting structure and a cascode configuration. In an I/O application the gate of the cascode transistor is tied directly to a power supply connection.

FIG. 73 is a schematic of an embodiment that does not require a quiet power supply. For a small amplitude signal, as

in RF signal applications, the drain to gate coupling of M1 will not turn on the channel of M1. Under this condition a quiet power supply is not required, allowing M2 of FIG. 71 to be eliminated. In this embodiment the pad is coupled to a silicon substrate through the N-well capacitance of diode CR2. The PMOS capacitor M3 of FIG. 71 is replaced by a metal capacitor that reduces total n-well area coupled through CR2. The configuration further reduces pad capacitance while still allowing gate boosting of shunting transistor M1 during an ESD discharge.

The details of ESD protection are disclosed in more detail in U.S. Patent Application No. 09/483,551 filed January 14, 2000 (B600:34208) entitled "System and Method for ESD Protection" by Agnes N. Woo, Kenneth R. Kindsfater and Fang Lu based on U.S. Provisional Application No 60/116,003 filed January 15, 1999; U.S. Provisional Application No. 60/117,322 filed January 26, 1999; and U.S. Provisional Application No. 60/122,754 filed February 25, 1999; the subject matters of which are incorporated in this application in their entirety by reference.

IF AGC AMPLIFIER

The VGA and PGA/LNA have characteristics in common that allow interchangeability in alternative embodiments.

FIG. 74 is a block diagram of a variable gain amplifier ("VGA") 3403. The VGA produces a signal that is a reproduction of a signal input to it at an amplified level. The amplified level in a VGA is capable of being varied. A variable gain is accomplished through the use of one or more control signals applied to the amplifier.

VGAs are frequently used to maintain a constant output signal level. VGAs do this by varying the amplifier gain to compensate for varying input levels. In the case of strong or weak signals it is desirable to maintain a linear gain for input verses output signals with little noise added. Maintenance of

a linear gain reduces distortion for high level input signals. VGAs are often used in IF or RF strips to compensate for prior losses or weak signal reception.

In a linear gain, a 1 dB increase in sinusoidal input signal level produces a 1 dB change in the output signal level at that same frequency. A gain of this nature is termed a "linear response." If a 1 dB change is not produced, this is indicative of an available power being diverted to produce a signal at another frequency of operation. A signal at a frequency other than desired often interferes with the signal being amplified and is termed distortion. Thus, the linearity of an amplifier is a figure of merit, the greater the linearity the better the quality of the amplifier. Amplifiers that utilize compensation circuitry and differential signal transmission tend to have improved linearity.

VGA compensation circuitry controls V_{ds}. For a large input signal, linearity and low gain is required. With a reduction in V_{ds}, good linearity and low gain are achieved. If a small signal is input to the amplifier, V_{ds} is increased. The increase in V_{ds} causes one or more MOSFETs internal to the VGA to be biased in the active region. Active region bias allows for high gain and low noise to be achieved simultaneously. The VGA utilizes a current steering method of applying control signals to provide an extended gain range VGA. The control of V_{ds} allows the production of a linear output when a large signal is applied to the input.

The VGA has a differential input comprising two signals, $+V_{in}$ and $-V_{in}$ 7408. The VGA has a differential current output comprising two signals, $+I_{out}$ and $-I_{out}$. In the embodiment shown the differential current signals are applied to a first and second resistor R1 and R2 to produce a differential voltage output, $+V_{out}$ and $-V_{out}$ 7410 respectively. Equivalently the

current outputs may be applied to work against any impedance to generate a voltage output.

A set of three control signals 7404 are supplied to the VGA 3403 from a linearization circuit 7402. The linearization circuit 7402 produces the three control signals 7404 that are derived from a single control signal, V_c 7406 through compensation circuitry. Control signal V_c tends to be proportional to the gain desired in the VGA 3403. The three control signals 7404 control the VGA in a manner such that a desired gain and a desired linearity tend to be produced by the VGA.

The linearization circuit is stimulated by the control signal V_c 7406 is supplied by an external DSP chip. The control signal applied to the linearization circuit 7402 is shaped in a predetermined way. A goal of shaping the control circuit is to produce the second set of control signals 7404 that are applied to the VGA 3403 to produce a desired VGA gain transfer function, measured in decibels, that changes linearly with the applied control signal V_c. In the embodiment shown V_c is a voltage, however a control circuit may be equivalently supplied. In an alternate embodiment the overall transfer function of the VGA is configured to yield a linear function of gain as measured with linear units versus control voltage by appropriately adjusting the linearization circuit through the application of a log to linear conversion current.

In addition to shaping the gain transfer function, another function of the linearization circuit is to control signals that control the VGA to produce the desired low distortion output. The second set of control signals 7404 are shown as a bussed line 7404. The second set of control signals comprise a voltage VD1, and a pair of control currents: iSig and iAtten. The second set of control signals 7404 tend to produce a linear change in gain

with variation of the control signal while maintaining an acceptable distortion level in the VGA.

The three control signals are generated by two subcircuits in the linearization circuit: a current steering circuit and a drain voltage control voltage signal generation circuit. The current steering circuit produces two signals, iSig and iAtten. The drain voltage control signal voltage generation circuit produces one signal, VD1.

FIG. 75, is a block diagram of the internal configuration of the VGA and the linearization circuit. The VGA and linearization circuit to implement current steering and V_{ds} control of the VGA are described as a separate function block. However, the functions described may be equivalently merged into the circuit functional blocks of the other.

The VGA 3403 is constructed from two cross coupled differential pair amplifiers 7500 7502. A first differential pair amplifier 7500 includes two transistors M4 and M10. A second differential pair amplifier 7502 includes transistors M13 and M14. The first and second differential pair amplifiers are driven in parallel by a differential input voltage 7408. When referenced to ground, the differential input voltage applied to each amplifier simultaneously is denoted $+V_{in}$ and $-V_{in}$.

The differential pair amplifiers have differential current outputs +I1, -I1, +I2, -I2, that are combined to produce a differential VGA output comprising $+I_{out}$ and $-I_{out}$. The first differential pair amplifier 7500 has differential current outputs +I1 and -I1 that are sinusoidal and 180 degrees out of phase from each other. The second differential pair amplifier 7502 has differential current outputs +I2 and -I2 that are sinusoidal and 180 degrees out of phase from each other. VGA output current $+I_{out}$ results from the combination at node 7505 of out of phase currents -I1 and +I2. VGA output current $-I_{out}$ results from the combination at node 7507 of out of phase currents +I1 and -I2.

Note that the currents described above having a minus sign prefix, -I1, -I2, are generated in response to input voltage $-V_{in}$, and the currents with plus sign prefixes, +I1, +I2, are generated in response to $+V_{in}$.

A V_{ds} control circuit 7504 within the VGA 3403 supplies a V_{ds} control voltage that is applied to nodes 7505 and 7508. The V_{ds} control circuit receives an input VD1 from a VD1 control signal generation circuit 7510 that is a part of the linearization circuit 7402. In alternative embodiments the V_{ds} control circuit is merged into the VD1 control signal generation circuit 751.

A current steering circuit 7512 in the gain control circuit 7402 supplies control signals iSig and iAtten. The signal iSig is a control input to the first differential pair amplifier 7500. The signal iAtten is a control input to the second differential pair amplifier 7500.

In the embodiment shown the VGA 3403 is configured to operate at an IF frequency. However it is understood that the VGA may be configured, by appropriate component selection to function at any desired frequency. In an IF strip, the addition of a VGA maintains a constant IF output as the input varies. This is accomplished by adjusting the gain of the VGA. A VGA is useful in any situation where a signal presented to a circuit is of unknown or variable strength.

Functionally the VGA maintains a constant level at its output so that subsequent circuitry may be designed that tends to have better performance and less noise. In alternate embodiments, the variable gain amplifier may be used at RF or other frequencies to reduce signal level variations in a circuit. For example in an embodiment, a VGA 3403 as described may be used in the RF front end 3408 to control the RF signal level that is applied to a receiver 3402.

The overall gain of the VGA is attributable to the individual gain contributions of transistors M10 M4, M13 and M14

that produce a current gain. In an embodiment, the VGA voltage gain is set by providing resistance at the $+I_{out}$ and $-I_{out}$ terminals to establish a voltage output, and thus a voltage gain for the amplifier. The exemplary embodiment includes field effect transistors ("MOSFETs"). Equivalently, other transistor types may be substituted for the MOSFETs utilized in the exemplary embodiment. A pair of control currents iSig and iAtten and a control voltage VD1 are principally used to provide an extended range of available VGA gain and a linear in dB VGA amplifier transfer function that provides a desired linearity.

Two methods of gain control are utilized in the exemplary VGA. The first method is V_{ds} control that controls noise and linearity while reducing VGA gain when large signals are applied, the second is current steering that provides an extended range of available VGA gain. The set of three control signals 7404 include iSig, iAtten and VD1.

In the first method of V_{ds} control, gain and linearity in the output of the VGA tend to be controlled by adjusting each of four transistors' M4, M10, M13, M14 drain source voltages ("V_{ds}") of the transistors to control a transductance ("g_m") associated with each transistor. If a drain source voltage V_{ds} across a MOSFET device M10, M4, M13, M14 is reduced, a g_m transfer characteristic of that transistor, which is a function of input voltage, becomes flatter. The flatter the g_m transfer function the more linearly the transistor tends to operates. The V_{ds} of all four transistors is controlled in order to manipulate an overall g_m characteristic for the VGA.

The V_{ds} gain control method tends to reduce VGA output distortion by tending to improve the linearity of the VGA. To improve the linearity, the V_{ds} of the transistors are reduced yielding better linearity in conjunction with a transistor operating point on a flattened g_m curve. As an input signal's strength increases, V_{ds} is reduced providing a linear response

VGA. Reducing V_{ds} also tends to contribute to VGA gain control. For small input signals as V_{ds} is increased the MOSFETs become biased in the active region where high gain and low noise operation is obtained. The main effect of reducing V_{ds} tends to be control of the linearity of the VGA amplifier.

In the second method, current steering control, currents iSig and iAtten tend to set amplifier gain over a large range. An increase in the control current iSig tends to increase gain by causing an increase in overall amplifier g_m, while an increase in iAtten tends to decrease gain by causing a subtraction of overall amplifier g_m. For certain type and size MOSFETs, the relationship between iSig, iAtten and g_m is as shown in equation (14)

$$g_m = \sqrt{\frac{K}{2}}\left(\sqrt{iSig} - \sqrt{iAtten}\right) \qquad (14)$$

where

iAtten = I_{tot} - Isig

K = a constant of proportionality

For other size/type transistors this relationship may not hold, but the idea is still applicable. The g_ms of each transistor M10, M4, M13, M14 is controlled to adjust gain. This is accomplished by subtracting, or adding currents through control lines iSig and iAtten to boost or reduce the VGA g_m, as required. Control signals iSig and iAtten control amplifier gain by adjusting an overall g_m of the amplifier. A fixed available control current is available for controlling VGA gain through the iSig and iAtten control lines. Gain is controlled by selectively steering the available current into the appropriate control line. For large VGA signal inputs, the linearity produced in a VGA from

current steering tends to be improved by the addition of the V_{ds} control circuit.

A single stage VGA amplifier with linearization circuitry as described above that utilizes current steering and V_{ds} control could yield a gain control range in excess of 40 dB.

The second method of VGA gain control is V_{ds} control. Linearity in amplifier output tends to be improved by V_{ds} control or "V_{ds} squeezing." With current steering, no provision is made for improving linearity once the input signal becomes large.

Linearity is typically determined by the g_m of each of the two differential amplifier stages. The first stage comprises M10 and M4. The second stage comprises M13 and M14. The embodiment described tends to have an increased linearity of 26 dB, corresponding to a factor of 20 improvement in linearity over that typically available.

VGA operating conditions determine the distribution the currents iSig and iAtten. When a small signal is applied to the input terminals $+V_{in}$ and $-V_{in}$, it is typically desirable to amplify the signal with a high gain setting. Transistors M10 and M4 are coupled to the differential output so that their g_ms tend to contribute to VGA overall gain. However, transistors M13 and M14 are coupled to the VGA output so that their g_ms tend to decrease VGA gain through a g_m subtraction. Transistors M4 and M10 are controlled by iSig, transistors M13 and M14 are controlled by iAtten.

For a high gain condition, g_m subtraction is undesired.

Thus, for a high gain setting, it is desirable to have most of the gain available from devices M10 and M4 contributing to the amplifier's overall gain. M10 and M4 are set for maximum gain by setting iSig to a maximum current. Correspondingly iAtten is set to a low value of current. In achieving a maximum gain, a control current is divided between iSig and iAtten such that a maximum current is present in the iSig line.

In the low gain state, the second differential pair transistors M13 and M14 are controlled by iAtten such that they subtract from the gain of M10 and M4. A large gain present for devices M13 and M14 creates a large gain subtraction in devices M10 and M4 which are controlled by iSig to produce a minimum gain.

Thus, when the signal input is small, minimum gain on M13 and M14 is desired and maximum gain on M10 and M4 is desired to produce maximum VGA gain. When the input signal is large, a maximum gain on M13 and M14 is desired and minimum gain on M10 and M4 is desired to produce minimum VGA gain.

FIG. 76 is a graph of gain versus the control current iSig. Control current iSig is shown as a fraction of iAtten, with the total current being equal to 1, or 100%. At the far right of the graph, a 0 dB reference is set corresponding to maximum amplifier gain of maximum amplifier g_m. As iSig is reduced, control current iAtten is increasing proportionately causing the VGA's overall g_m and gain to decrease.

Maximum VGA gain is desirable with a small input signal present at the VGA input. Maximum gain is achieved with a maximum current into the iSig control line and minimum current into the iAtten control line. As the signal at the VGA input becomes larger, it is desired to decrease the amplifier gain. A reduction in VGA gain is achieved by decreasing the current in the iSig line and increasing the current in the iAtten control line. A minimum VGA gain corresponds to maximum current in the iAtten control line and minimum current into the iSig line.

Returning to FIG. 75 ,the linearization circuit takes the externally supplied control signal 7406 that is provided as a voltage and converts it to control signals 7404 that are current and voltage signals. In the current steering circuit 7512 a maximum control signal voltage amplified in the embodiment described corresponds to a maximum gain condition with iSig set

to a maximum and iAtten being set to a minimum. As the control voltage is decreased, iSig decreases and iAtten increases.

The control voltage Vc 7406 is created by digital circuitry that is responsive to the input level of the amplifier. In the embodiment described the gain control loop is closed in a digital circuitry domain located off of chip that produces control signal 7404.

The output of the VGA is sampled to determine if sufficient signal strength is available for further signal processing. The sample is processed by an A to D converter into a digital signal, and the control voltage responsive to the level of the VGA output is created. Alternatively, analog methods may be used to sample the output and generate control voltage. In an embodiment the VGA is utilized as an IF VGA. In alternate embodiments the VGA is configured for used at other frequency bands that require an adjustment in gain.

Stability of the AGC loop is maintained during changes in iSig and iAtten. Stability is achieved in the minimum gain setting by keeping iSig greater than iAtten. In the embodiment described iSig is prevented from becoming less than iAtten by the linearization circuit. If iSig becomes less than iAtten, phase inversion problems tend to occur causing a degradation in VGA performance, disrupting automatic gain control ("AGC") loop performance in a receiver. This condition is prevented from happening by providing appropriate circuitry in the linearization circuit.

Also with respect to AGC loop stability, a zero gain setting is undesirable. In the embodiment, the transistors are fabricated with identical dimensions, and it is possible to set the gain equal to zero by making the iSig and iAtten currents equal. This is undesirable from a control loop stability standpoint. The linearization circuit provides appropriate circuitry preventing this condition from occurring.

Maximum attenuation is determined by how close iSig is allowed to approach iAtten in value. Thus, the maximum attenuation achieved is dependent upon the stability that is permissible as iSig approaches iAtten.

FIG. 77 is the schematic diagram of an embodiment of the VGA. The VGA has a control circuit to control the V_{ds} of M10 and M13 at node 7505, and the V_{ds} of M4 and M14 at node 7507.

A control voltage VD1 is generated by the linearization circuit 7510 and applied to control a differential amplifier U1. The negative input of U1 is coupled to node 7505, and the positive input of U1 is coupled to node 7507.

A transistor M1 has its source coupled to node 7505, its drain comprises the $+I_{out}$ terminal of the VGA. The gate of transistor M1 is coupled to the positive output of U1. A transistor M2 has its source coupled to node 7507, its drain comprises the $-I_{out}$ terminal of the VGA. The gate of transistor M2 is coupled to the negative output of A1.

The V_{ds} squeezing is utilized since it tends to improve linearity. As the control signal voltage increases, the control voltage VD1 decreases tending to decrease the VGA gain. As previously discussed, iSig is decreasing and iAtten is increasing to achieve the desired decrease in VGA gain. Concurrently with V_{ds} squeezing, the V_{ds} of all four transistors M10, M4, M13, M14 also tends to decrease with increasing input signal level due to the application of a variable DC voltage at the transistor source leads. A DC voltage is fixed at nodes 7501 and 7503. Thus, the way available to reduce V_{ds} for M10, M4, M13, and M14 is to reduce the DC voltage at the $+I_{out}$ and $-I_{out}$ terminals. A variable voltage source is connected at each node $+I_{out}$ and $-I_{out}$ - 7505, 7507.

The sources of M13 and M14 are coupled in common to node 7503 and to the control signal iAtten. Control signal iAtten tends to cause a decrease in amplifier gain, while control signal

iSig tends to increase amplifier gain. The sources of M10 and M4 are coupled in common to iSig at node 7510. The drains of M10 and M13 are coupled in common to provide an output signal $+I_{out}$. The drains of M4 and M14 are coupled in common to provide an output signal $-I_{out}$. In the exemplary embodiment input $-V_{in}$ is coupled to the gates of M10 and M14. Input $+V_{in}$ is coupled to the gates of M4 and M13. In the exemplary embodiment differential inputs and outputs are shown in the amplifier. However, it is understood by those skilled in the art that a single ended configuration is equivalently produced by the use of a device such as a balun.

FIG. 78a illustrates a family of curves showing the relationship of a transistor's drain current ("I_d") to its gate source voltage ("V_{gs}") measured at each of a series of drain source voltages ("V_{ds}") from 50 mV to 1 V. From this graph a transconductance, g_m is determined. The following relationship defines a g_m curve for each V_{ds} value:

$$g_m = dI_d \setminus dV_{gs} \qquad (15)$$

FIG. 78b is a graph of g_m verses V_{gs} as V_{ds} is varied from 50 mV to 1 V. To provide improved output linearity performance, it is desirable to operate a transistor on a curve of g_m that has a constant value and zero slope. As seen in the graph for a V_{ds} of approximately 50 mV, the curves of g_m verses V_{gs} tend to be flat. As V_{ds} is increased, the curve begins to slope, indicating the presence of non-linearity in the output signal. As V_{ds} increases the curve not only begins to slope, but it develops a bow, further complicating the compensation for the non-linearities at the higher level of V_{ds}. These irregularities in g_m tend to be the sources of non-linearities in the output of the amplifier. Thus, it is desired to provide a flat g_m response to

produce a more linear transfer function for the VGA by controlling V_{ds}.

FIG. 78c is a graph of the cross-section of FIG. 78b plotting g_m verses V_{ds} for various values of V_{gs}. As V_{ds} changes from approximately 200 mV to 500 mV, g_m changes from approximately 5 mS to 13 mS. The change in g_m from 5 mS to 13 mS by changing V_{ds} may be used to control gain. Thus, as V_{ds} is decreased, the gain is decreased. Control of V_{ds} provides approximately 9 dB of gain control range.

Within the range of V_{ds}, graphed between the vertical bars 7801, the value for g_m remains essentially the same for a range of V_{ds} input signal from 1.2 V to 1.4 V. Thus by controlling V_{ds} from 200 mV to 600 mV approximately 9 dB of gain control is provided.

When control of V_{ds} is combined with the g_m subtraction method previously described, the linear output signal is maintained. In addition approximately 8 dB to 9 dB of gain control in addition to that provided by g_m subtraction contributes to provide overall VGA gain control on the order of 30 dB, in the exemplary embodiment.

Output linearity is often quantitized by measuring an intermodulation product produced by two input signals present at differing frequencies (f_1 and f_2 302 and 304 respectively of FIG.3). For the VGA a two tone intermodulation ("IM") product test is utilized, and the distortion as represented by the third order intermodulation product (308 of FIG. 3) is measured. Approximately a 26 dB decrease in the third order IM product (308 of FIG. 3) tends to be achieved in the exemplary embodiment.

With the input signal maintained at a constant level, the output signal at $+I_{out}$ and $-I_{out}$ is measured as gain squeezing is performed. Improvement is measured as compared to adjusting gain without utilizing gain squeezing. A reduction in third order intermodulation of approximately 25 dB is measured as V_{ds} is

squeezed within a range of approximately 150 mV to 200 mV. Utilizing a test having two tones at 44 MHz and 45 MHz typically produces third order intermodulation product components at 43 MHz and 46 MHz. With this test, 20 dB to 25 dB improvement in third order intermodulation is observed in the exemplary embodiment. A typical improvement of 20 dB is realized in the linearity of the output signal.

FIG. 79 is a schematic of a current steering circuit. An external control signal V_c drives a differential pair amplifier 7910 including MC1, MC2, to ultimately generate iSig and iAtten. The iSig and iAtten are generated through two current mirrors 7904, 7906. The first current mirror 7904 comprises MC3 and MC6. The second current mirror 7906 comprises MC4 and MC5. The circuit maintains a fixed relationship between iSig and iAtten, defined by:

$$I_{tot} = iSig + iAtten \qquad (16)$$

To guarantee that phase reversal does not occur, iSig must remain greater than iAtten at all times. By selecting V_{ref} to be slightly less than the minimum value of control voltage V_c that will be present, iSig will remain greater than iAtten.

In an embodiment of current steering circuit 7512, a control voltage V_c is applied to a differential pair amplifier 7910. In the exemplary embodiment, control signal V_c ranges from 0.5 V to 2.5 V. The 0.5 V corresponds to a minimum gain setting and 2.5 V corresponds to a maximum gain setting. Differential pair amplifier 7910 comprises two transistors MC1 and MC2. In the exemplary embodiment, field effect transistors are used. Equivalently, other types of transistors may be substituted for field effect devices. The inputs to the differential pair amplifier are the gates of MC1 and MC2. The sources of MC1 and MC2 are coupled in common to a current source I_{tot}. Current

source I_{tot} is in turn coupled to a supply voltage V_{cc}. Current source I_{tot} is conventional current source constructed as is known by those skilled in the art.

The drains of MC1 and MC2 are coupled to current mirrors 7904 and 7906, respectively. Control voltage V_c is coupled to the gate of MC1 and a voltage reference is coupled to the gate of MC2. Voltage reference V_{ref} is typically constructed as conventional voltage source known to those skilled in the art. The currents present in the sources of MC1 and MC2 drive current mirrors 7904 and 7906, respectively. Current mirror 7904 comprises transistors MC6 and MC3. Current mirror 7906 comprises transistors MC4 and MC5. These current mirrors are constructed conventionally as is known by those skilled in the art. Output of current mirror 7904 and 7906 consists of the control signals iAtten and iSig.

FIG. 80 is a schematic of a VD1 control signal generation circuit. Control signal V_c is fed to the positive input of a differential amplifier U2. Signal ended output of amplifier U2 is fed into the gate of transistor MC9. The source of MC9 is connected to the negative input of U2. The source of MC9 is also coupled to a first terminal of a resistor R1. A second terminal of R1 is coupled to ground. The drain of MC9 receives a current i_{c1} that is supplied by a drain of transistor MC7. The drain of MC7 is coupled to the gate of MC7. The source of MC7 is coupled to a supply voltage V_{cc}. The gate of MC7 is coupled to the gate of MC6. The source of MC6 is coupled to a supply voltage V_{cc}. The drain of MC6 is coupled to a first terminal of a resistor R2. The second terminal of resistor R2 is coupled to node 1001. The node formed by coupling MC6 to R2 supplies control signal VD1. Together transistors MC7 and MC6 form a current mirror 8001.

Control current V_c sets up the control current i_{c1} through amplifier U2, resistor R1 and transistor MC9. Current i_{c1} is mirrored through transistor MC7 and MC8 of the current mirror.

The current generated in the drain lead of MC6 creates a voltage across resistor R2 as reference to the voltage present on node 7501. Thus, R1 and R2 are sized properly to control V_{ds} across M10, M4, M13 and M14. For example, VD1 can range from 100 mV to 600 mV. This condition corresponds to a V_c = 05V at a minimum gain maximum input condition and a V_c = 2.5V maximum gain minimum input signal condition.

In alternative embodiments, control voltage V_c may be subjected to conditioning by temperature compensation circuitry and linear in dB transfer function compensation before being applied to the VD1 generation circuit 7510.

The details of VGAs are disclosed in more detail in U.S. Patent Application No. 09/547,968 filed April 12, 2000, (B600:36598) entitled "Large Gain Range, High Linearity, Low Noise MOS VGA" by Arya R. Behzad; based on U.S. Provisional Application No. 60/129,133 filed April 13, 1999 (B600:34440), the subject of which is incorporated in this application in its entirety by reference.

DIGITAL IF DEMODULATOR

An integrated receiver such as is shown in FIG. 48 converts a received signal down to an intermediate frequency, suitable for a final down conversion to one or more base band signals by an IF demodulator. It is desirable to integrate the IF demodulator onto a silicon substrate to the maximum extent possible, and to also include the receiver on a common substrate with the IF demodulator. It has been difficult to integrate a receiver and an IF demodulator due to the large number of external components previously needed.

However, a digital IF demodulator, utilizing digital signal processing techniques to implement the IF demodulator functions allows integration of the demodulator into a single substrate. When an integrated tuner such as is described in FIG. 48 and the

accompanying text is disposed upon the same substrate as the digital IF demodulator a low cost circuit that converts a high frequency signal to a base band signal is possible. With the digital IF demodulator the added benefit of providing programmability to allow demodulation of multi-standard video signals with a single tuner is possible.

FIG. 81 is a block diagram of a typical prior art IF demodulator 8013. A demodulator is typically cascaded after a RF tuner (or synonymously, a receiver) 4822. The RF tuner typically converts an RF carrier signal, impressed with a modulated signal, at a first frequency to an IF signal at a second carrier frequency impressed with the modulated signal. The second carrier frequency, or IF is typically lower in frequency than the RF signal. Alternatively, the receiver may be of the direct conversion type that produces an output that consists solely of the modulated signal without a carrier.

It is desirable to integrate a tuner and IF demodulator onto a single substrate 8017 to reduce parts count, cost and size. Typical substrate materials suitable for RF integrations are often costly and result in incomplete integrations. It is desirable to integrate a tuner and demodulator onto a single low cost silicon substrate fabricated with the low cost CMOS process. However, complete integration onto a single low cost substrate is difficult to achieve because limitations of the designed circuitry often call for external components in a typical tuner and IF demodulator circuit.

Between the tuner and IF demodulator, a filter 8003 is often present, as well as a variable gain amplifier 8015. The variable gain amplifier is shown as part of the demodulator circuit block 8013, however it is commonly implemented as a stand alone module. The filter 8003 and variable gain amplifier 8015 may be associated with either the tuner circuitry of the IF demodulator circuitry.

Typical external circuitry utilized in an analog IF demodulator is an audio band pass filter 8009, a Nyquist filter 8003 having a controlled slope for vestigial sideband (VSB) demodulation, a PLL loop filter 8007 and a VCO tank circuit 8005. The external circuitry typically requires components having values that do not facilitate integration onto a single substrate. Large values of capacitance or inductance often required in tuned circuits tend to be large and difficult to integrate satisfactorily on a substrate. In addition these components are difficult to tune, or adjust to utilize a single tuner in various applications. A tuner that allows digital programmability of circuit parameters to allow the tuner to be used in differing applications would be desirable.

For example, an inductance often present as a coil tends to be utilized in tank circuits 8005, and filters 8009 and 8003. Inductance is often fabricated by forming a spiral conductor on an integrated circuit substrate. The spirals are typically lossy and large, an inefficient utilization of integrated circuit layout area. Tuning of an integrated inductor is typically not performed.

Large values of capacitance typically found in filter design tend to utilize large integrated circuit areas to provide a separation of charge required to provide a given capacitance. Changing values of integrated capacitance is typically accomplished with banks of switched capacitors. Thus, by providing a circuit including the previously described tuner 4822 that minimizes or eliminates external circuit components with a IF demodulator circuit that tends to minimize or eliminate external circuitry a space efficient and economical integrated circuit may be fabricated. An exemplary tuner circuit may be as previously described in the text accompanying block 4822 of FIG. 48.

FIG. 82 is a frequency spectrum of a typical NTSC television signal. Television signals typically utilize vestigial-side band (VSB) transmission. In a typical television channel, three carrier frequencies are typically utilized to transmit a picture with sound. The carriers include a picture carrier 8202, a color carrier 8207 and a frequency modulated (FM) sound carrier 8215. The color carrier and picture carrier utilize vestigial side band (VSB) modulation.

A vestigial side band modulated signal comprises an amplitude modulated signal having two side bands 8209, 8211 in which one of the side bands has been partially suppressed 8209. The suppressed side band is termed a vestigial side band 8209. VSB modulation is desirable since it requires less frequency spectrum than an AM modulated signal to transmit the same information.

An AM modulation also known as double side band (DSB) requires twice the band width of a single side band (SSB). In AM modulation the two side bands and carrier are present. In SSB one side band is present and the carrier is suppressed. The carrier is present in the VSB signal.

A single side band receiver typically requires complex circuitry, while an AM receiver is simple to construct. VSB transmission is a compromise between the AM and SSB transmission. Thus, the vestigial side band modulation is a compromise that allows a simpler receiver to efficiently utilize the band width of a television channel.

A typical television signal incorporates carriers that transmit audio 8216, color 8203, 8205 and monochrome 8201 signals. Each signal is typically impressed upon a subcarrier. The manner of modulating desired information onto each of the subcarriers varies with the type of transmission standard or modulation being used. For example, in the NTSC system, the sound signal 8216 is impressed upon a subcarrier 8215 through

frequency (FM) modulation. The video signals 8213, including the monochrome 8201 and color information 8203, 8205 are each impressed upon sub-carriers 8202, 8207. The color information is further encoded before it is impressed upon its sub-carrier. The color sub-carrier utilizes phase and amplitude quadrature modulation to interlace two color signals 8203, 8205 on the color sub-carrier 8207.

In the vestigial side band picture signal information present from approximately DC to 1 MHz is repeated in the vestigial side band 8209. If such a signal were processed by a conventional AM receiver. The low frequency video information would tend to have a voltage value of twice the high frequency video signals from approximately 1 MHz and above. This is because the low frequency information in the upper side band 8211 is repeated in the vestigial side band 8209.

The voltages of the received picture signal are typically made equal by utilizing an intermediate frequency (IF) band pass filter (BPF) that shapes the picture signal by attenuating frequencies from approximately 1 MHz from the picture carrier 8102 and below. A filter with the described pass band shape is termed a Nyquist filter. A typical IF BPF filter is a SAW filter, that shapes the pass band response. A saw filter is typically an external device since it is disposed on a pizeo-electric substrate such as zinc oxide. It is desirable to simplify the IF filter by utilizing an IF BPF with a flat response, that is integrated onto a substrate such as silicon.

FIG. 83 is a block diagram of an embodiment of a digital IF demodulator 8309. In the embodiment shown, the digital IF demodulator 8309 is disposed upon a substrate 8301. In the embodiment shown, the substrate is silicon fabricated according to the CMOS process. In alternative embodiments, different processes may be utilized.

The digital IF demodulator 8309 is typically disposed on a common substrate 8301 with a receiver circuit (not shown) that supplies an IF signal to the IF in port 8311. An exemplary receiver suitable for common integration is the receiver shown in FIG. 48. In an alternate embodiment, the digital IF demodulator 8309 is disposed on a common substrate 8301 with additional analog signal processing circuitry including as inputs, signals A, C, A prime, and S from the digital IF demodulator 8309. In further alternative embodiment, an RF receiver (not shown) is coupled to the digital IF demodulator 8309 which is in turn coupled to analog signal processing circuitry (not shown) and is disposed on a common substrate 8301. In a further alternative embodiment, the digital IF demodulator 8309 and a receiver coupled to the digital IF demodulator are disposed upon a common substrate 8301 with a conventional transmitter circuit (not shown) operating in cooperation with the digital IF demodulator, for example to establish a two way communications path in a communications system.

The digital IF demodulator 8309 typically includes an input section 8308 in which analog signals input to the digital IF demodulator are processed and converted from the analog to the digital signal domains. Signals from the analog input section 8308 that have been converted into digital signals are further processed by digital single processing block 8305. In the digital single processing block 8305 DSP techniques are utilized so that conventional analog circuit functions are fabricated with digital signal processing circuitry. DSP circuit elements advantageously allow digital programmability of the parameters of each circuit such that a high degree of flexibility in using and programming the digital IF demodulator is possible such that input signals formatted to various standards may be accommodated.

In I^2C Control bus 8307 is disposed upon the substrate 8301 and couples digital control lines to the digital signal processing functional blocks 8305 allowing them to be programmed. The I^2C bus also provides control to the analog input section 8308 and an analog output section 8303.

Analog output section 8303 is disposed on the common substrate 8301 and converts digital signals from the DSP block 8305 into analog signals suitable for further processing by subsequent analog single processing circuitry.

In the embodiment shown, the digital IF demodulator demodulates NTSC video signals that are impressed upon an IF carrier frequency and input to the digital IF demodulator 8309 at the IF port 8311. The signal at input IF IN is fed into a variable gain amplifier (VGA) 8317. An exemplary VGA is described in FIG. 74. The output of the variable gain amplifier 8317 is coupled to the input of a conventionally constructed analog to digital converter (ADC) 8319, where an analog IF signal is converted to a digital signal. The digital output of ADC 8319 is coupled to a conventionally constructed AGC peak detection circuit 8315, and also to a conventionally constructed VIF demodulator and Nyquist filter 8321.

The AGC peak detection circuit 8315 implements an analog circuit function in digital circuitry utilizing conventional digital signal processing techniques. The AGC peak detection circuit provides two outputs used to control automatic gain control in the tuner. Tuner automatic gain control is available by establishing a connection at the pad labeled RF AGC. A second AGC peak detection output is conventionally converted with the DAC 8313 into an analog control signal utilized to control the IF level. The IF level is controlled by applying a second AGC peak detection control circuit to the analog voltage control input of voltage controlled amplifier 8317. The AGC peak detection circuit 8315 examines the magnitude of the number

representing the IF level output from analog to digital converter 8319 to generate the two AGC outputs proportional to that level. In an alternative embodiment, the AGC peak detection circuit is implemented as an analog circuit having an input sampled at the IF output of VGA 8317. In the alternate embodiment, DACs 8311 and 8313 are eliminated since the analog AGC peak detection circuit provides analog outputs.

The AGC peak detection circuit 8315 output is fed into a conventionally constructed digital to analog converter circuit 8311 where the digital signal is converted into an analog signal that is output as a signal named RF AGC. The AGC peak detection circuit 8315 also outputs a signal to a conventional digital to analog converter 8313. The analog output of digital to analog converter 8313 is supplied as an output AGC TP and simultaneously as a control signal input to an analog variable gain amplifier 8317. Typically coupled to AGC TP is a filter capacitor to low pass filter the DAC 8313 output. DAC outputs 8313 and 8311 are control currents that cause the gain of the variable gain amplifiers they are coupled to increase or decrease.

An analog to digital converter (ADC) 8319 is coupled to the output of the VGA 8317. The output of the ADC 8319 is coupled to AGC peak detection circuit 8315, and an input of a VIF demodulator and Nyquist filter 8321.

FIGS. 84a-84d are frequency spectra showing digital VIF demodulation and Nyquist filtering of an exemplary received band of television channels received at an IF frequency and presented to the VIF demodulator and Nyquist filter and the circuitry contained therein.

FIG. 84a is a frequency spectrum of an exemplary input signal to the VIF demodulator and Nyquist filter circuit (8421 of FIG. 83) as present at node 8349 of FIG. 83. A conventional analog to digital converter (ADC) 8319 disposed internally to the VIF demodulator and Nyquist filter is coupled to input node 8349

and provides a frequency conversion when operated in a sub-sampling mode. The illustrated spectrum is an analog representation of the digital signal present at input node 8349, since in block 8309 of FIG. 83 all of the signals exist as digital representations of analog values.

A typical receiver (not shown) has a bandwidth typically three channels wide allowing the three channels shown to pass through and be down-converted to an IF frequency as shown. For the NTSC television signal shown, a desired channel has a picture carrier at 44.75 MHz. A sampling frequency of an analog to digital converter (ADC), included in the VIF demodulator and Nyquist filter (8321 of FIG. 83), is chosen to be lower than the picture carrier frequency. The ADC sampling frequency is also selected to be lower than the lowest frequency present in the desired channel, such that aliasing problems typically encountered in the process of folding a signal down to baseband are not encountered.

FIG. 84b is an illustration of the output of the ADC converter. The frequency spectrum has been shifted down to a low IF frequency by the ADC converter operated in the sub-sampling mode. The signal is then coupled to a digitally implemented Nyquist filter.

FIG. 84c illustrates a spectra output of a Nyquist filter. A digital Nyquist filter is coupled to the sub-sampling ADC. Digital filtering is used to implement a filter having a slope characteristic of a Nyquist filter. By choosing the ADC sampling frequency at the edge of the IF saw filter passband, the tuner acts as an additional image filter, and the image channel is strongly attenuated before it folds on top of the desired channel.

The picture carrier is positioned such that its frequency falls at the midpoint in frequency of the Nyquist filter's characteristic slope. The picture carrier is utilized as a

synchronous demodulation signal. An accurate Nyquist slope is typically needed to prevent folding half of the frequency band into the baseband. Thus, the Nyquist filter truncates the desired channel and removes the image channel and any other channels present in the spectrum.

FIG. 84d is a frequency spectra showing the resultant shift from the low IF frequency of FIG. 84c to baseband. In mixing the desired channel down to baseband, the picture carrier is utilized as the local oscillator (LO) signal. With the picture carrier or LO falling partially in band with the desired channel, part of the channel is caused to fold back on itself after the mixing process. The Nyquist filter slope is selected such that when the channel folds back on itself, the constant output level of the desired channel is maintained across its frequency bandwidth.

Returning to FIG. 83, the output of the VIF demodulator and Nyquist filter 8421 is coupled to an automatic frequency tuning (AFT) circuit 8323. The AFT circuit provides a feedback signal coupled to the tuner (not shown) to adjust a local oscillator of the tuner.

Output of the AFT 8323 is a digital signal that is coupled to digital to analog converter 8325 where it is converted back into an analog signal. The output of DAC 8325 is fed back to the tuner circuit (not shown). Implementation of the automatic frequency tuning circuit by digital signal processing techniques allows a more accurate automatic gain control for controlling a typical television receiver to be implemented.

The second output of the VIF demodulator and Nyquist filter 8421 is simultaneously coupled to three filters 8327, 8337, 8345.

A low pass filter 8327 is conventionally constructed according to digital signal processing techniques. Filters implemented utilizing digital signal processing techniques are typically programmable allowing the filter parameters to be varied through one or more programming lines. The output of the

first filter 8327 is simultaneously fed into a conventionally constructed sync detector and AGC circuit 8331 and into a second conventionally constructed digital variable gain amplifier 8329, constructed using DSP circuit design techniques.

The sync detector and the AGC circuit 8331 provide an output utilized as a control voltage to the second, or digital, VGA 8329 at a digital control signal control signal input. The output of the second VGA is coupled into a conventionally constructed digital to analog converter 8333. The analog output of DAC 8333 is coupled to a conventionally constructed buffer amplifier 8335. The output of amplifier 8335 forms the analog output labeled C.

Filter 8337 is a bandpass filter conventionally constructed utilizing digital signal processing techniques. This filter has the same degree of adjustability as described for filter 8327. The output of bandpass filter 8337 is fed into the input of a conventionally constructed FM demodulator circuit 8339. The output of the FM demodulator circuit is fed into a conventionally constructed digital to analog converter 8341.

In an alternative embodiment, digital to analog converter 8341 is a delta sigma type digital to analog converter. The output of digital analog converter 8341 is fed into a conventionally constructed buffer amplifier 8343. The analog output of buffer amplifier 8343 forms the A-prime output of the digital IF demodulator 8309.

Filter 8345 is a high pass filter. The high pass filter is constructed utilizing conventional digital signal processing design techniques. High pass filter 8345 possesses the same degree of programmability described for filter 8327. The output of filter 8345 is coupled to a conventionally constructed digital to analog converter 8347. The analog output of digital to analog converter 8347 forms output S of the digital IF demodulator 8309.

FIG. 85 is a spectrum of an NTSC television signal relative to the filter responses of filters 8327, 8337 and 8345. Low pass filter 8327, bandpass filter 8337, and high pass filter 8345 separate the second signal output of the VIF demodulator and Nyquist filter 8421 into three signal components.

Low pass filter 8327 passes the video signal represented by envelope 8507. The exemplary video signal includes a color subcarrier 8501 located at 3.57 MHz. The envelope of the low pass filter response 8509 allows passage of the video signal. In the exemplary NTSC signal, an FM sound carrier 8503 is present at 4.5 MHz. The bandpass filter response 8511 is designed to pass the first FM sound carrier. A second sound carrier typically encountered in high end television systems 8505 is passed by high pass filter response 8513.

Returning to FIG. 83, low pass filter 8327 passes video information and rejects sound carriers. Low pass filter 8327 is a digital circuit implemented utilizing digital signal processing techniques, such that the filter cut-off frequency and roll-off may be programmed externally. In addition, the digital filters are integrated onto the substrate 8301 as an integral unit that is part of the IF demodulator 8309.

The utility of the programmable filters is illustrated by the varying locations of the sound carriers. For example, in an NTSC signal, the sound carrier appears at 4.5 MHz. For PAL standards, the sound carrier appears at 5 or 5½ MHz. Thus, a demodulator utilizing programmable filters tends to process television signals processed according to differing formats, such as NTSC and the varying PAL standards. The output of low pass filter 8327 is coupled simultaneously to a second variable gain amplifier (VGA) 8329 and a sync detection and AGC circuit 8331. The sync detect and AGC circuit provides a clamping function and automatic gain control to control VGA 8329.

A composite video signal contains sync pulse information and varying video information. It is desired to clamp the black level of the picture to a desired output level. Thus, the black level and the amplitude of the sync signal are controlled by the sync detect and AGC circuit. A typical sync pulse is 250 mV. If the sync pulse is not approximately 250 mV, then the gain is appropriate controlled to achieve this level of sync pulse amplitude. The output of the second VGA 8329 is coupled to the input of a digital to analog converter 8333. The analog output of the DAC 8333 is coupled to a buffer amplifier 8335, having an output C available for further video processing.

Bandpass filter 8337 filters out the sound carrier. Typically this filter would have different characteristics depending upon which standard of television broadcast signal the digital IF demodulator is designed to process. However, with filters integrated in the digital domain, a multi-standard digital IF demodulator may be implemented by making the parameters of filter 8337 adjustable through digital programming. Digital programming may be accomplished through I^2C programming or by supplying discrete logic levels to the filter 8337. The output of bandpass filter 8337 is coupled to the input of an FM demodulator 8339. This circuit path demodulates one FM sound carrier. The FM demodulator 8339 is constructed from a digital PLL circuit that provides demodulation of the FM carrier. DSP implementation of the FM demodulator allows very large time constants to be provided in the loop filter without the need for large external components. The output of FM demodulator 8339 is coupled to a digital to analog converter 8341.

Digital to analog converter 8341 is a conventionally constructed DAC. In an alternative embodiment, a sigma delta DAC utilizing an oversampling function, including a noise shaping response, improves the signal to noise ratio in the final analog

audio output. The output of DAC 8341 is coupled to the input of a buffer amplifier 8343 having an output coupled to port A prime.

High pass filter 8345 is coupled directly to the input of DAC 8347, whose output is coupled to terminal S. This pathway provides unmodulated FM sound information at terminal S. A path such as through high pass filter 8345 would typically be used to pass multiple sound carriers, such as those utilized in dual language broadcasts. Alternatively, output S may be coupled to a surround sound system.